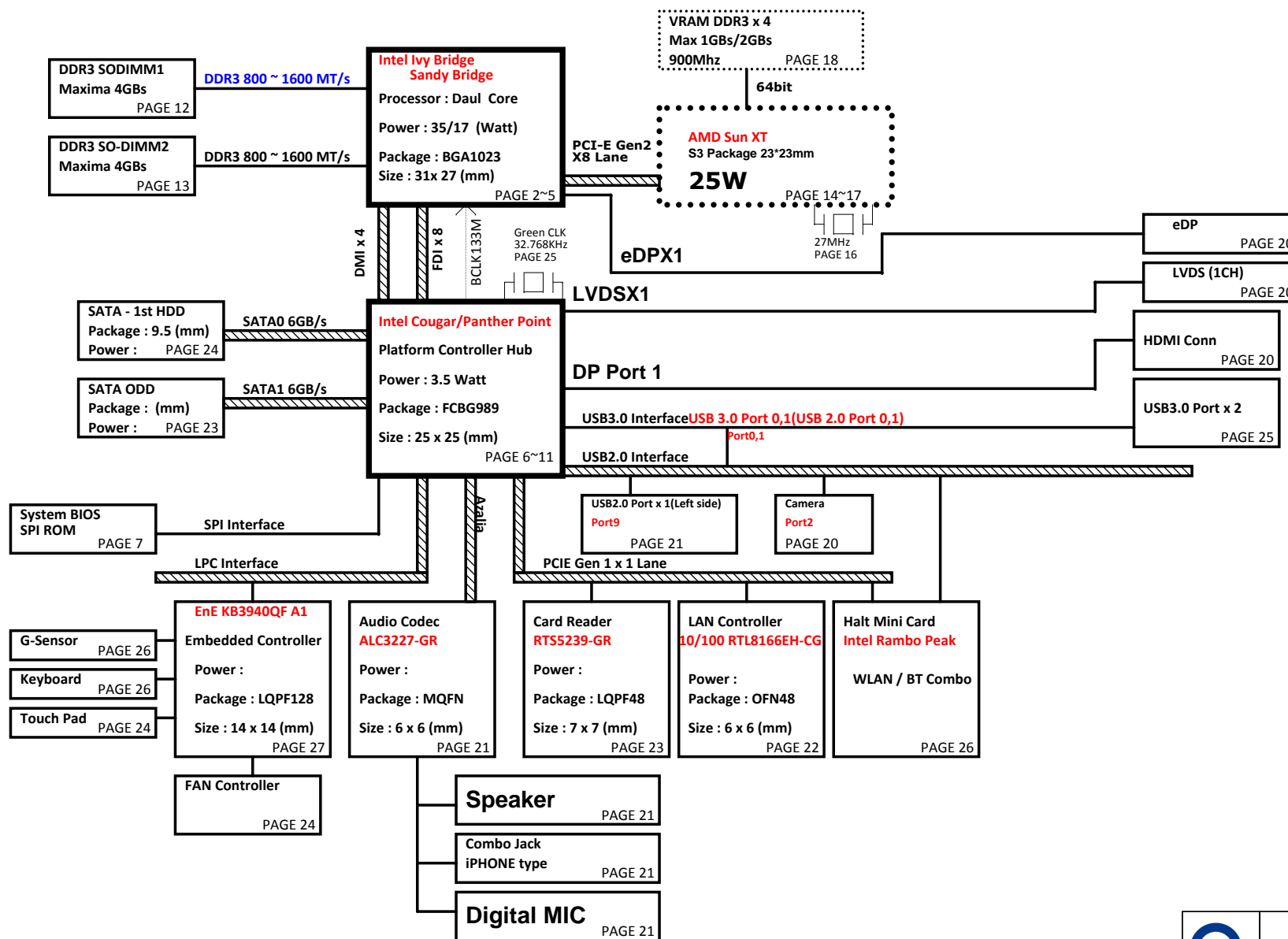


U81 DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

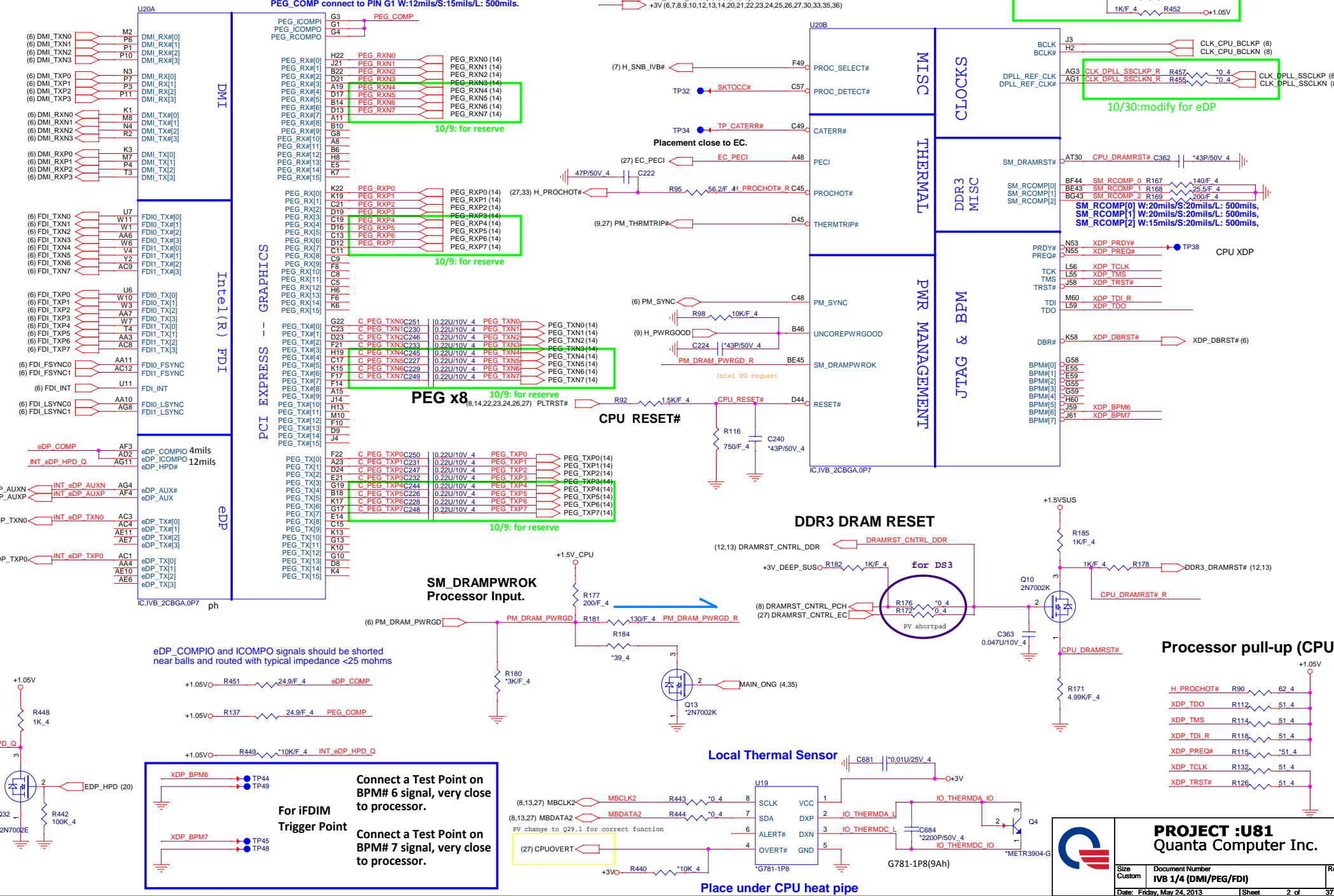


Ivy Bridge Processor (DMI,PEG,FDI)

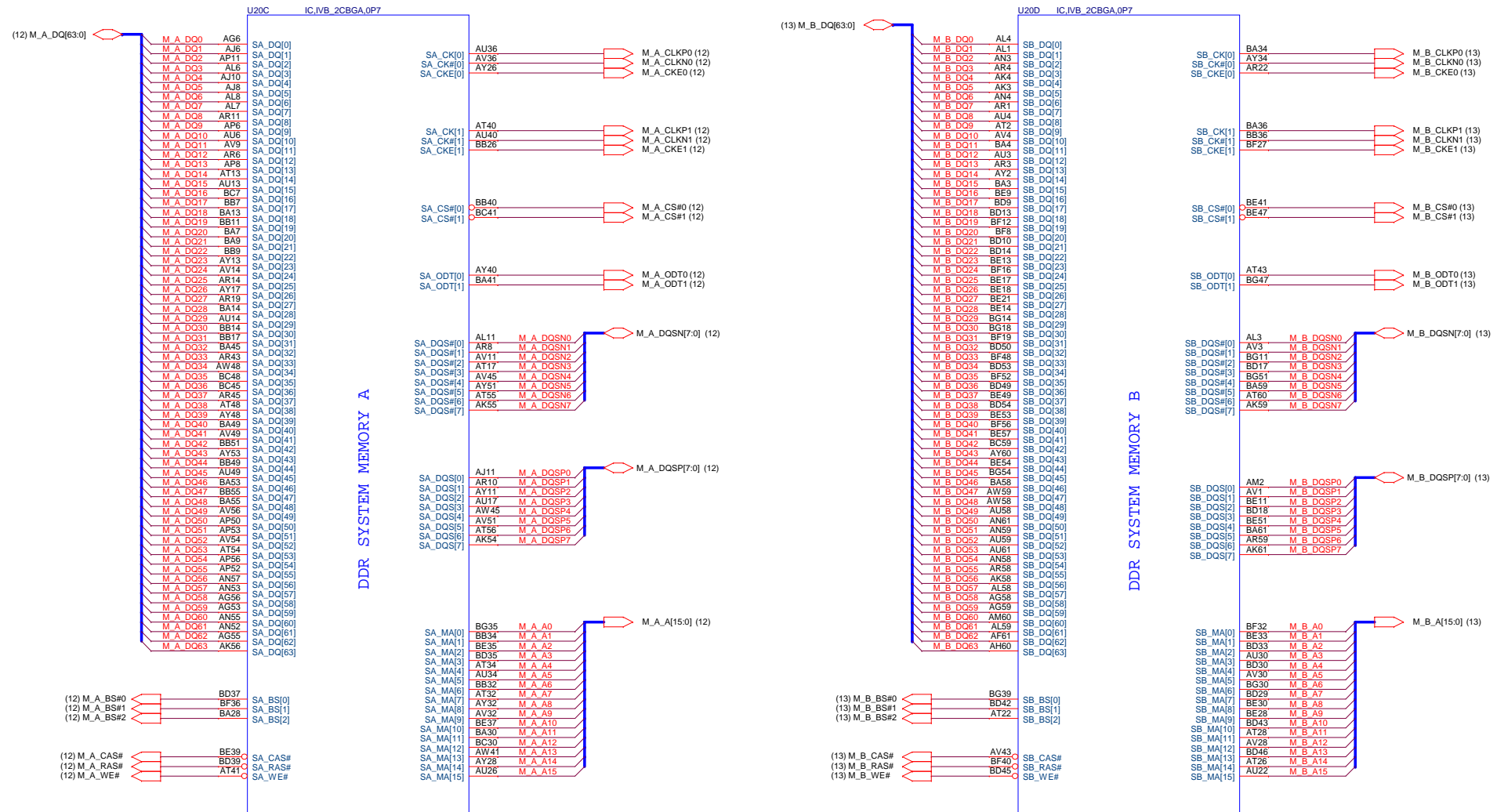
02

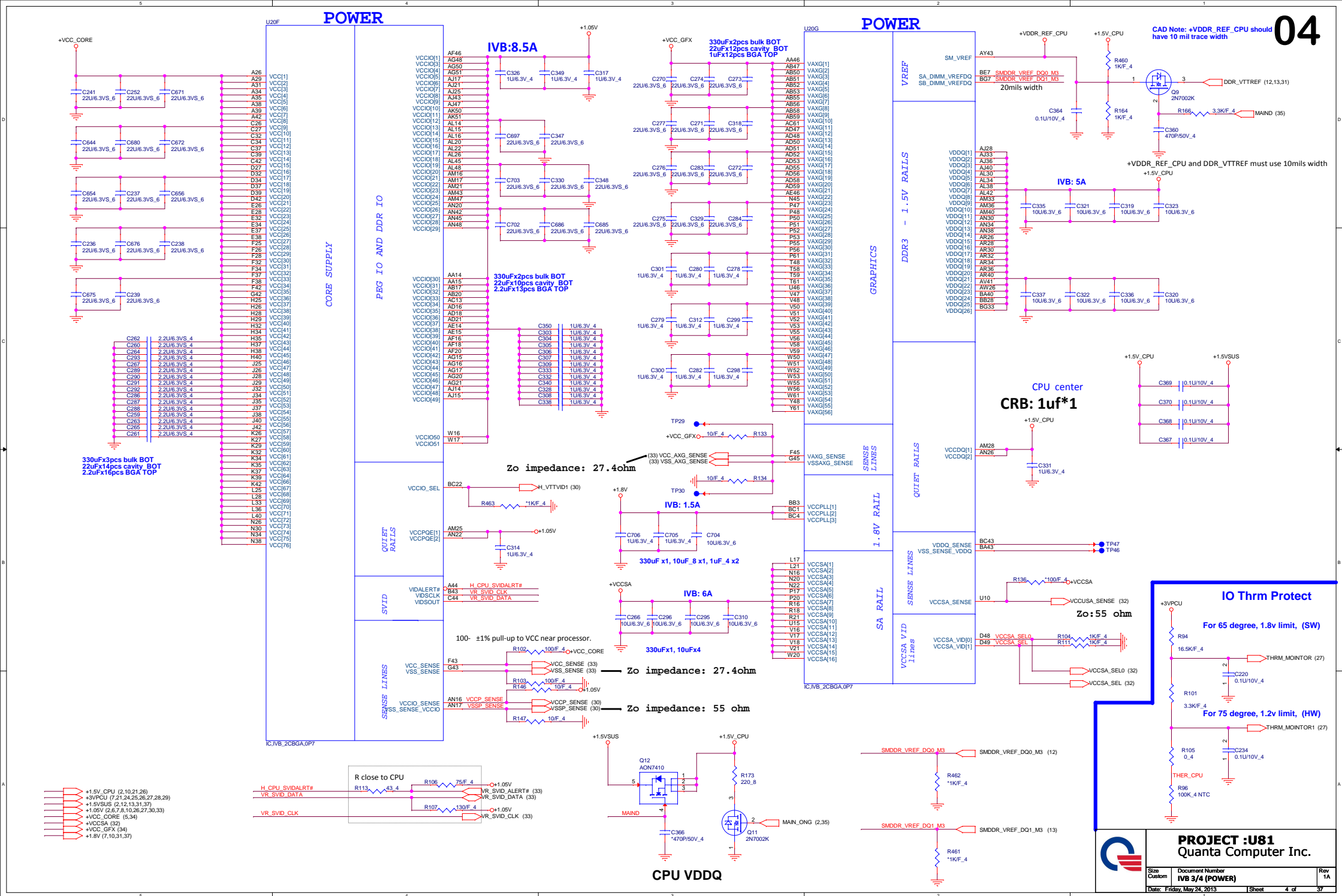
PEG_COMP connect to PIN G3/G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

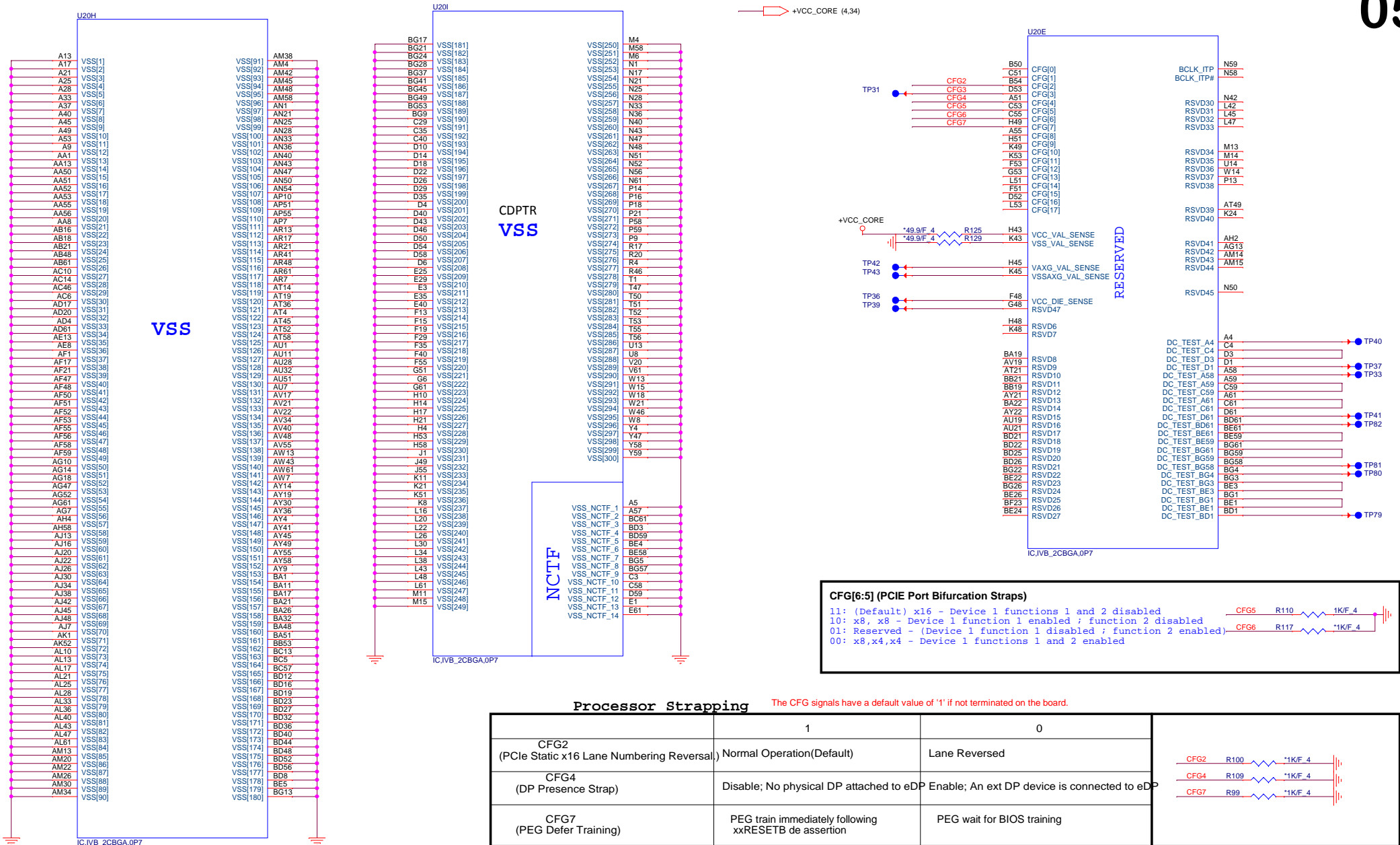
10/30:reserved for eDP



Ivy Bridge Processor (DDR3)

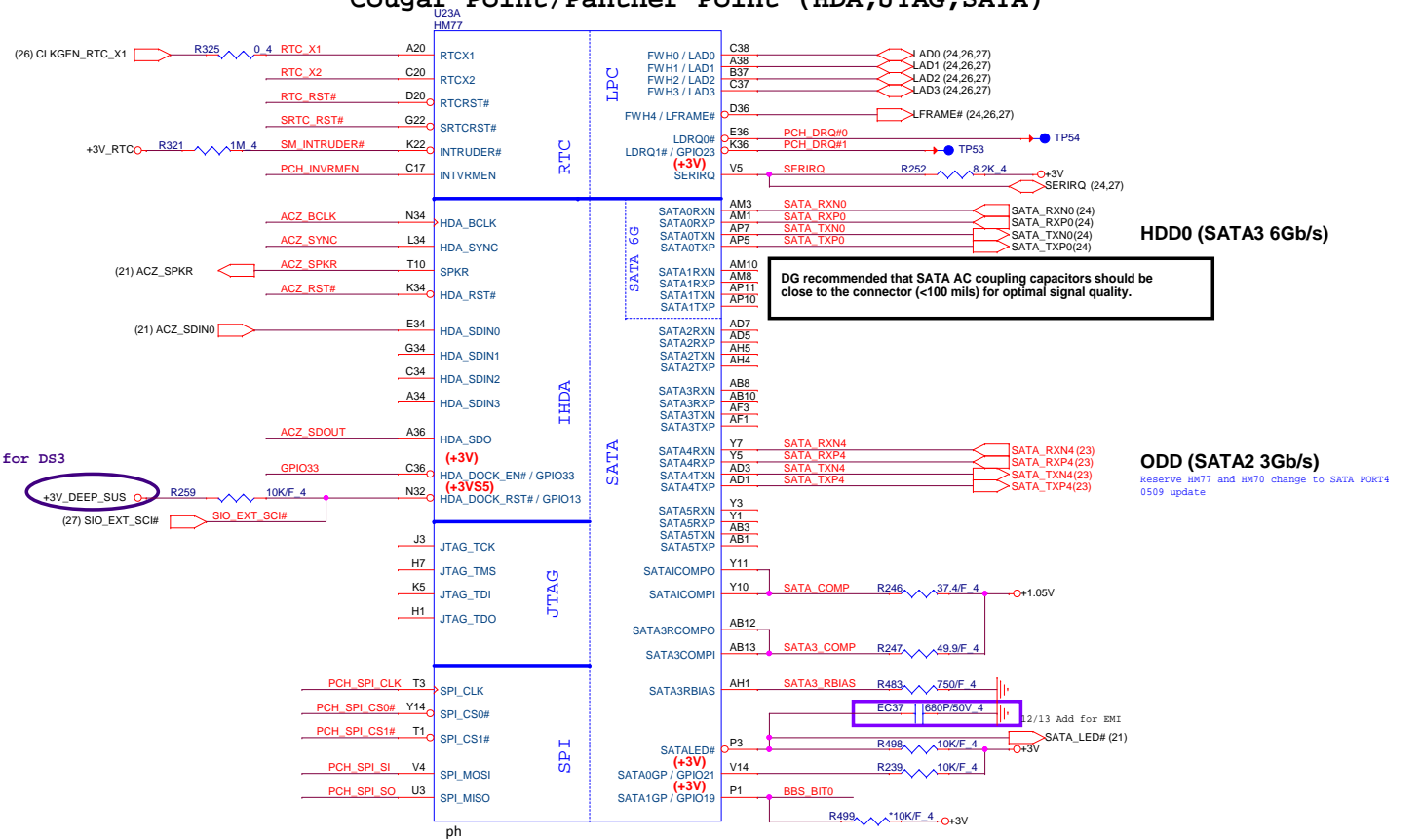






Cougar Point/Panther Point (HDA,JTAG,SATA)

07



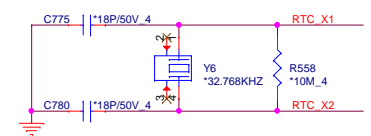
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

HDD0 (SATA3 6Gb/s)

ODD (SATA2 3Gb/s)

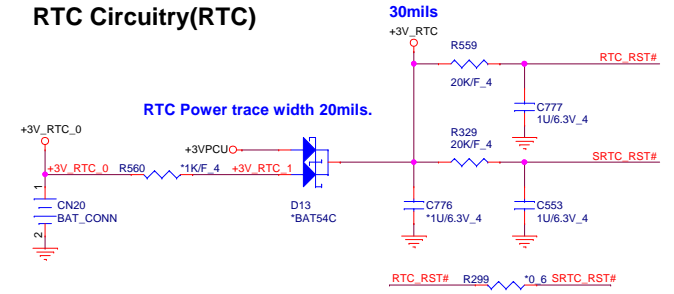
Reserve HM77 and HM70 change to SATA PORT4 0509 update

RTC Clock 32.768KHz

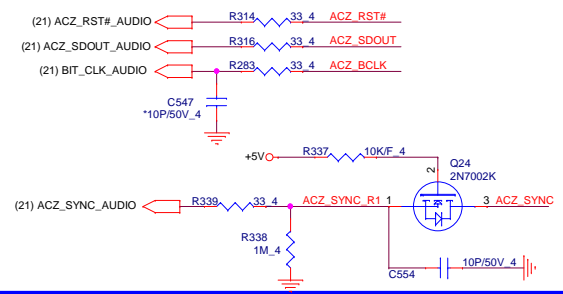


no stuff if use green Clock

RTC Circuitry(RTC)

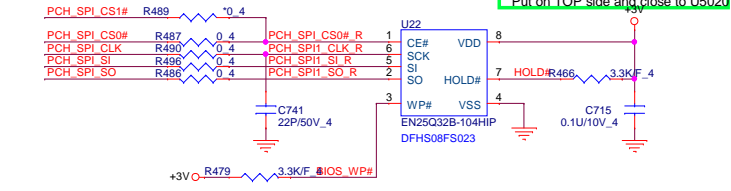
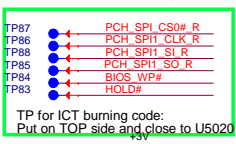


HDA Bus(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023(91960-0084L-8P-SOCKET)

PCH SPI ROM(CLG)



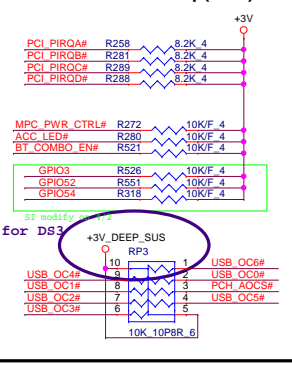
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R237 1K/F 4 ACZ_SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V ₀ R529 1K/F 4 PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V ₀ R320 330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	BIOS_WP# R471 0.4 GPIO33
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K		[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K		R502 1K/F 4 BBS_BIT0
GNT2# / GPIO53	ESI strap (Server only)	PWR0K	Should not be pull-down (weak pull-up 20K)	R517 1K/F 4 BBS_BIT1 (8)
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWR0K	0 = Disable (Internal pull-down 20kohm)	USE GPIO PIN
NV_CLE	DMI Termination voltage	PWR0K	weak pull-down 20kohm	+1.8V ₀ R472 1K/F 4 INV_ALE (8)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.8V	+1.8V ₀ R473 2.2K 4 R474 1K/F 4 INV_CLE (9) H_SNB_IVB# (2)
HDA_SDO	Flash Descriptor Security	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	+3V ₀ R479 3.3K/F 4 BIOS_WP#
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

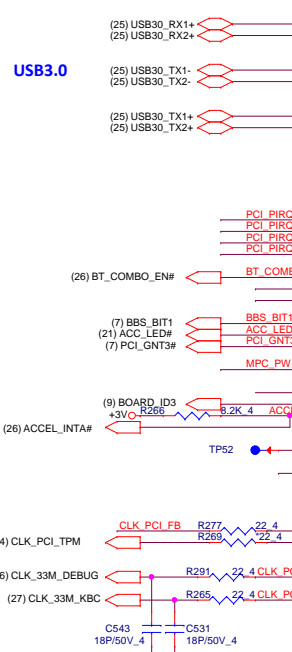
PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
Date: Friday, May 24, 2013	Sheet 7 of 37	

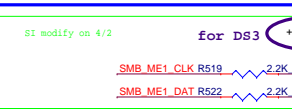
PCI/USBOC# Pull-up(CLG)



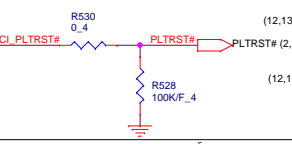
USB3.0



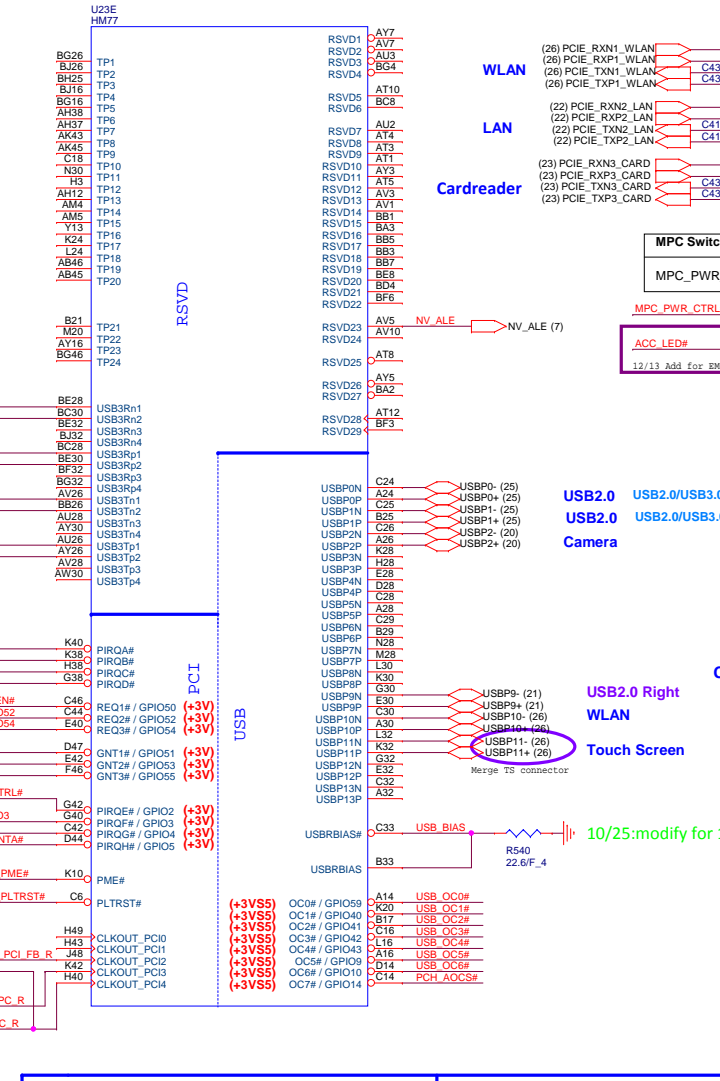
SMBus/Pull-up(CLG)



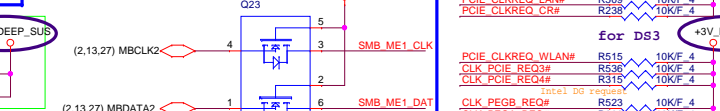
PLTRST#(CLG)



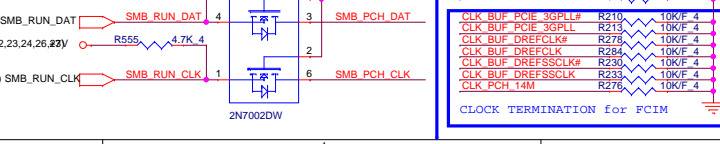
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



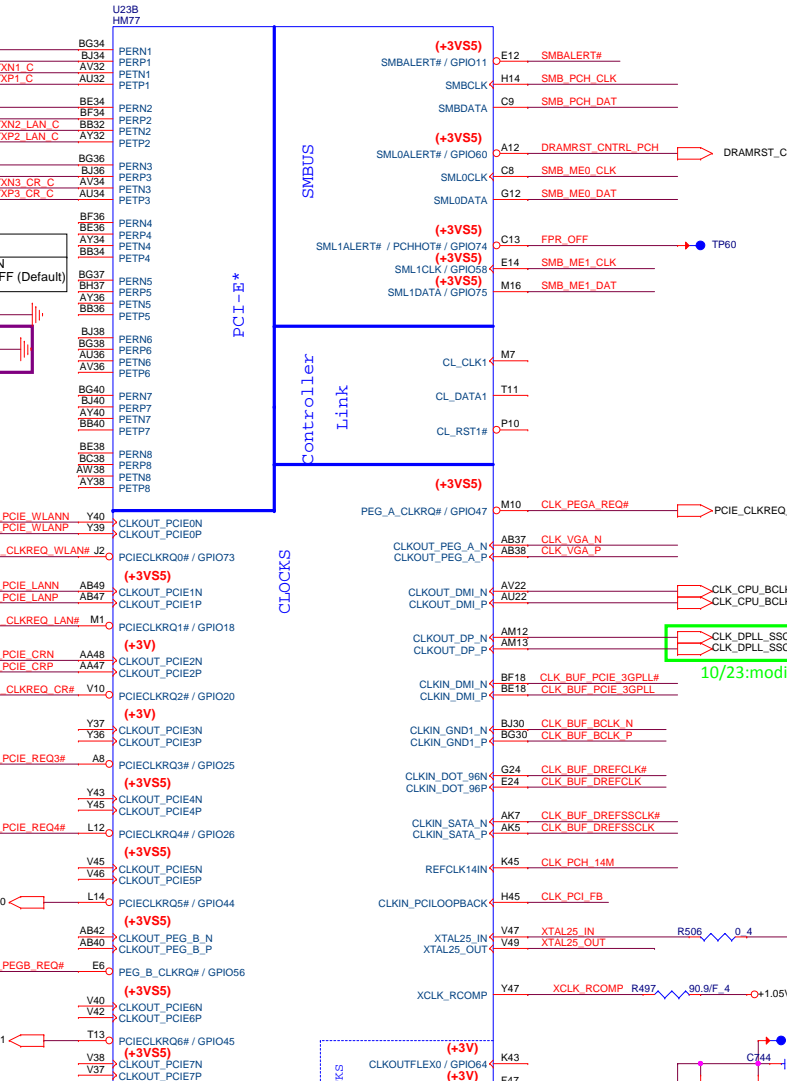
SMBus/Pull-up(CLG)



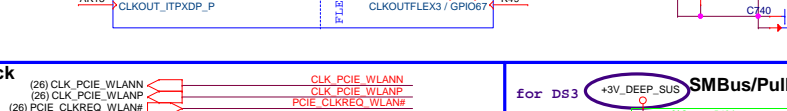
CLK REQ/Strap Pin(CLG)



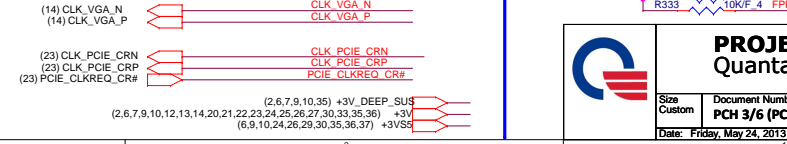
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



SMBus/Pull-up(CLG)



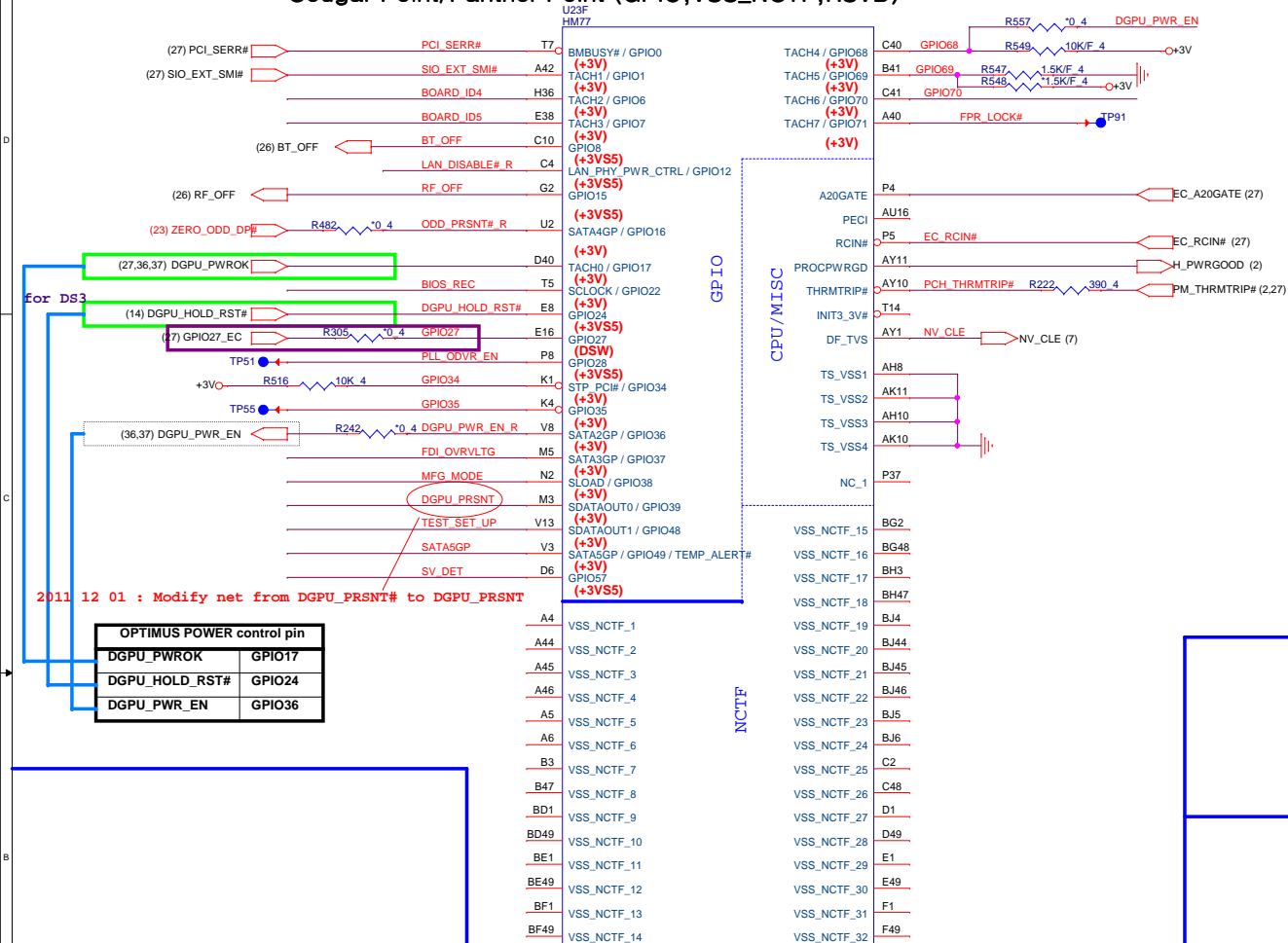
PCI Clock



PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number PCH 3/6 (PCI-E/USB/CLK)	Rev 1A
Date: Friday, May 24, 2013	Sheet 8 of 37	

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)

for D83

+3V_DEEP_SUS

MFG-TEST

MFG_MODE

Bios swap GPIO.

PCI_SERR#

for D83

+3V_DEEP_SUS

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

BIOS RECOVERY

High = Disable (Default)

Low = Enable

TEST_SET_UP

SV_SET_UP

High = Strong (Default)

R286

TEST DETECT

Low = Default

SATA2GP/GPIO36

Reserved only

R231

FDI_OVRVLTG

Reserved only

(2,6,7,8,10,12,13,14,20,21,22,23,24,25,26,27,30,33,35,36) +3V

(6,10,24,26,29,30,35,36,37) +3VSS

PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

Date: Friday, May 24, 2013 Sheet 9 of 37

Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
U81 UMA	0	0	0	0	0	0
U81 SWG	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0

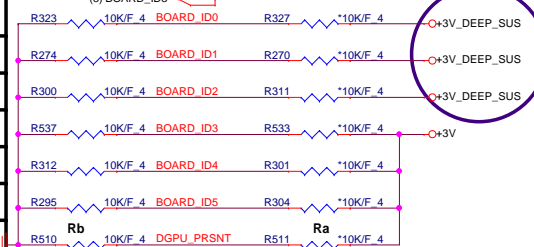
(8) BOARD_ID0

(8) BOARD_ID1

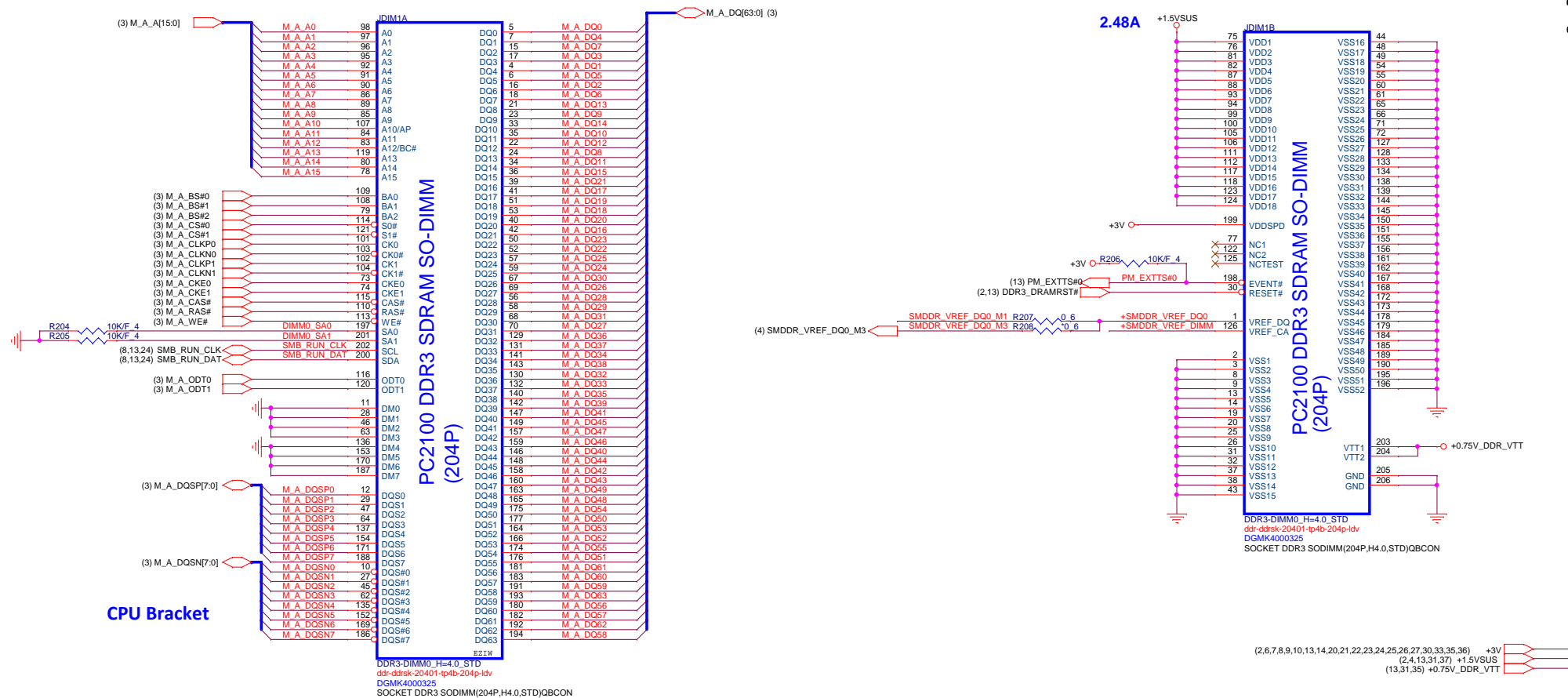
(8) BOARD_ID2

(8) BOARD_ID3

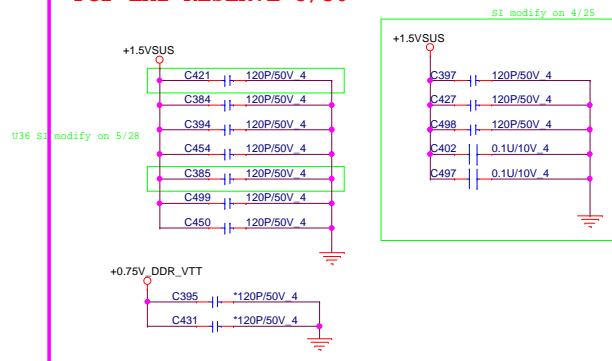
for D83



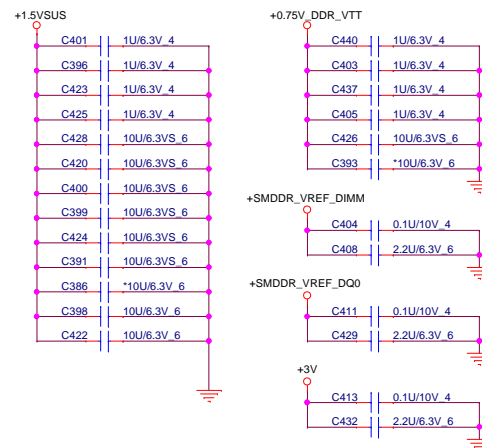
SG	UMA
Stuff	Ra
NC	Rb



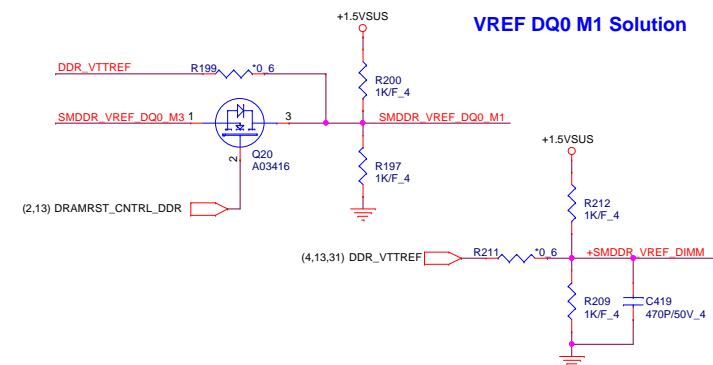
For EMI RESERVE 8/30

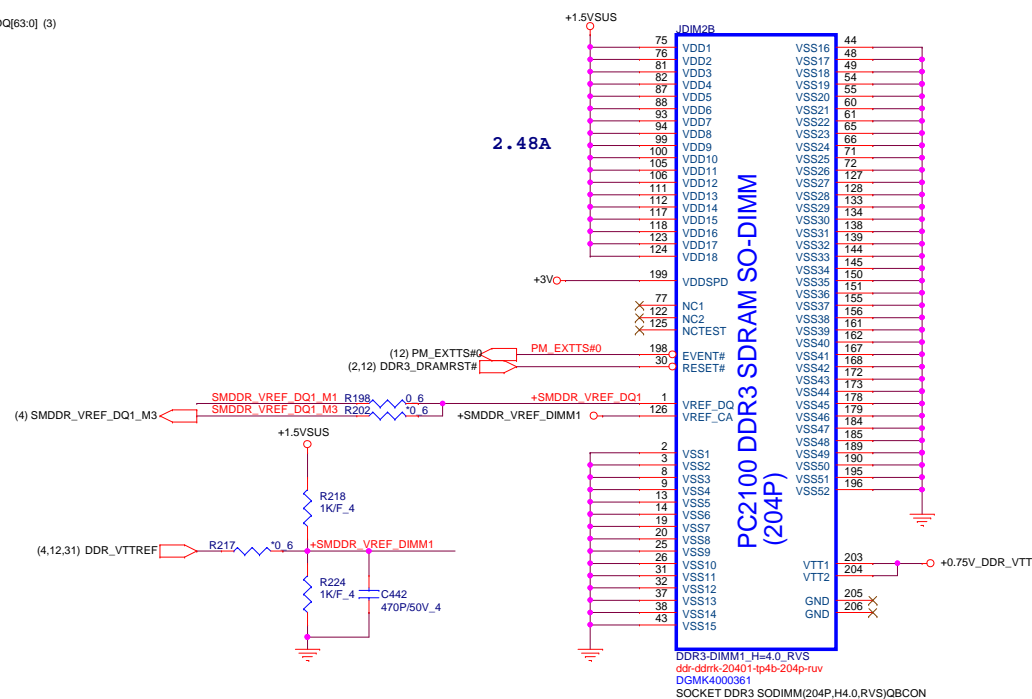
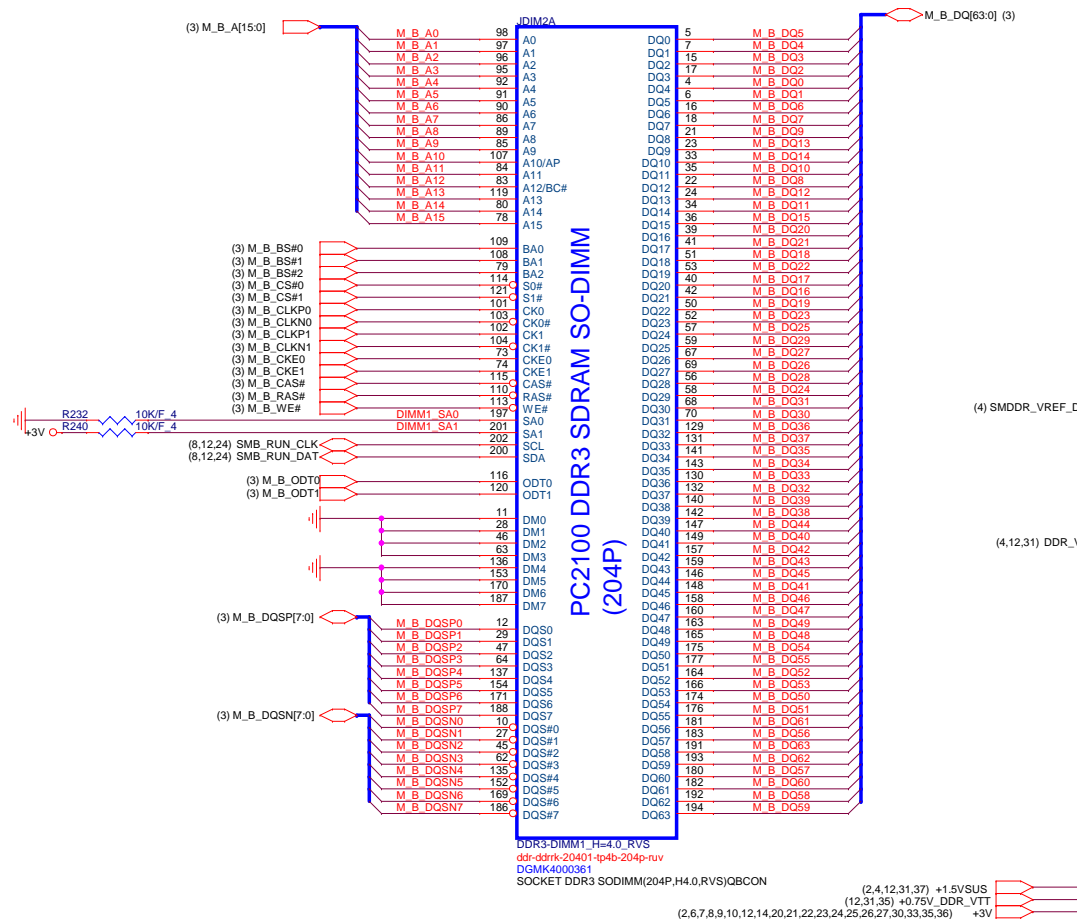


Place these Caps near So-Dimm0.

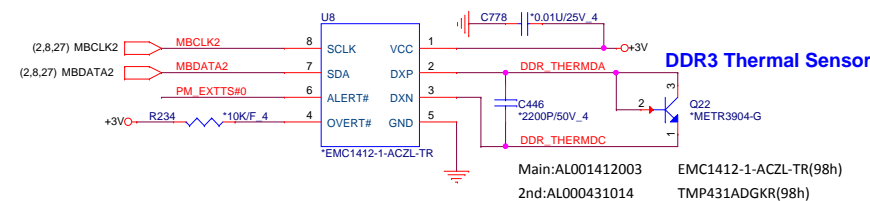


VREF DQ0 M1 Solution

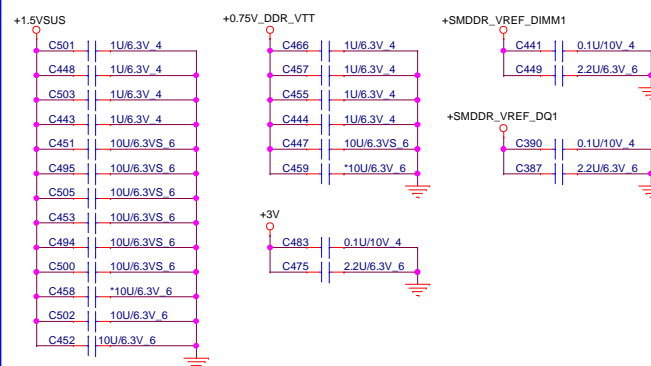




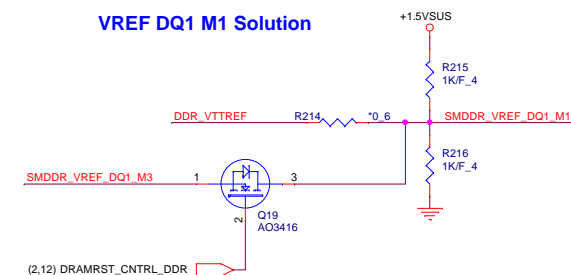
Local Thermal Sensor



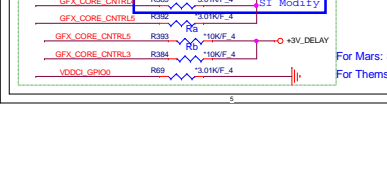
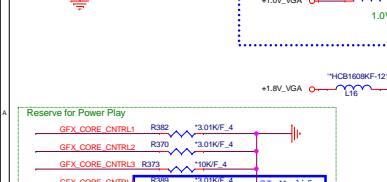
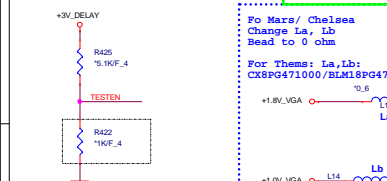
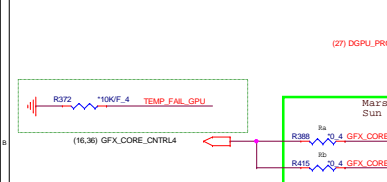
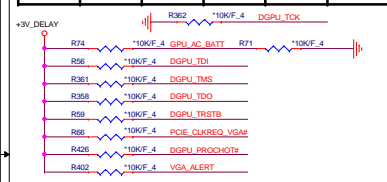
Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution

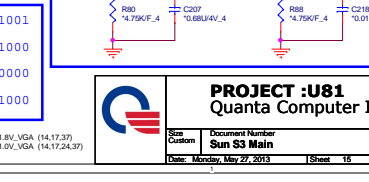
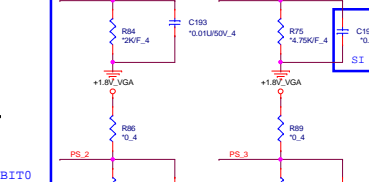
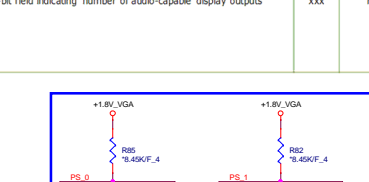
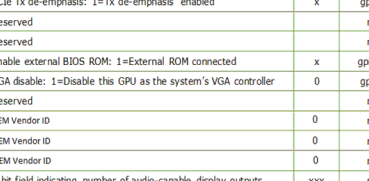
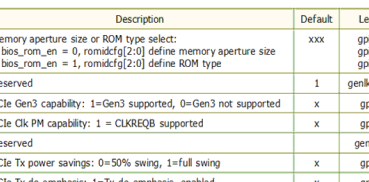
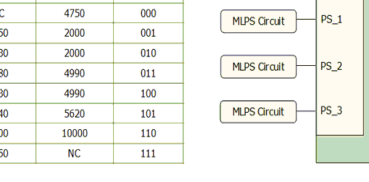
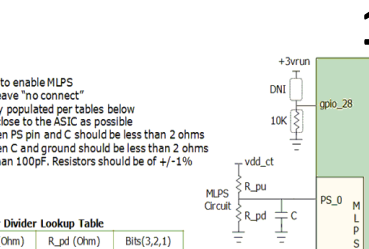
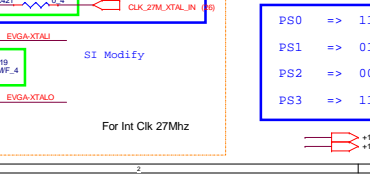
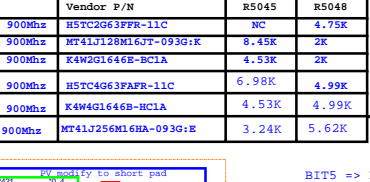
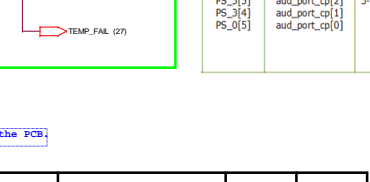
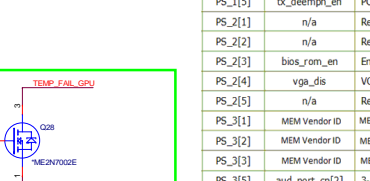
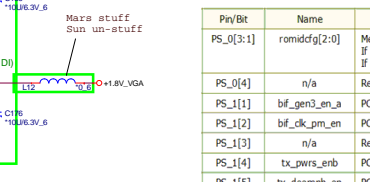
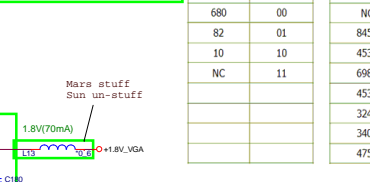
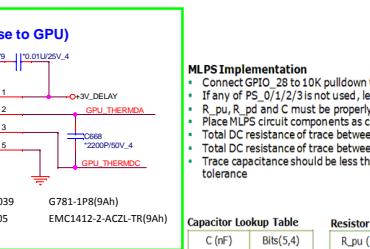
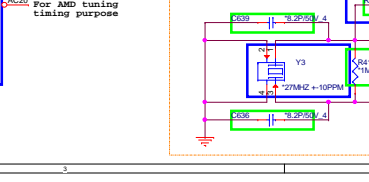
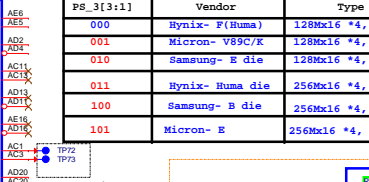
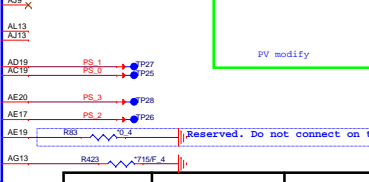
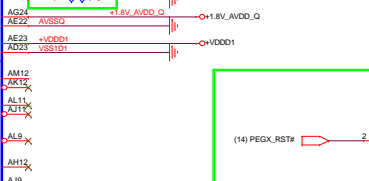
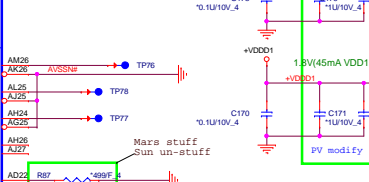
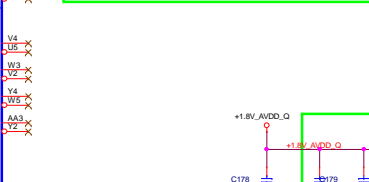
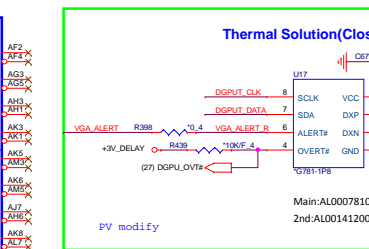
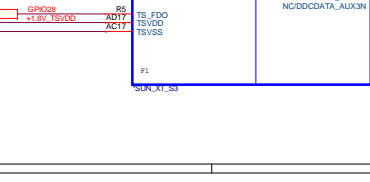
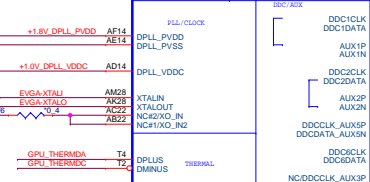
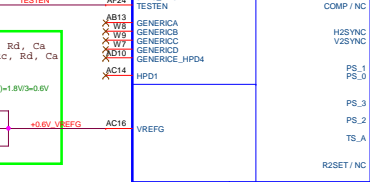
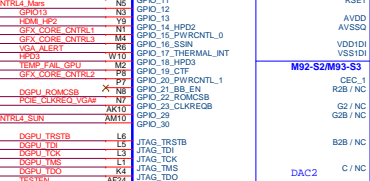
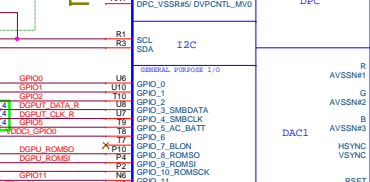
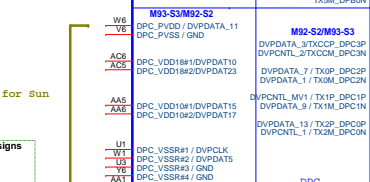
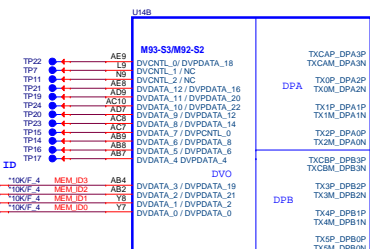
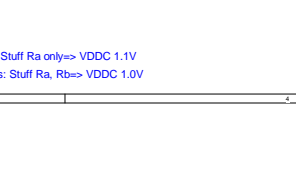
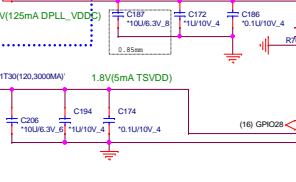
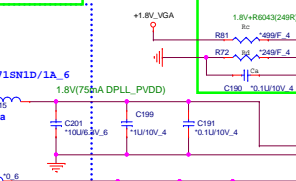
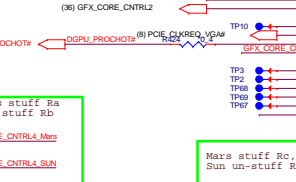
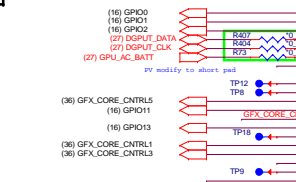
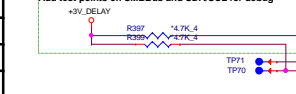


GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCTRL5	PWRCTRL4	PWRCTRL3	PWRCTRL2	PWRCTRL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V



Default

Access to SMBus are SDA/SCL is mandatory on all designs
Add test points on SMBus and SDA/SCL for debug



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

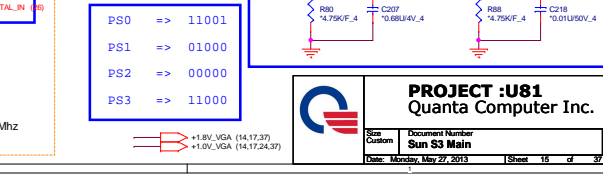
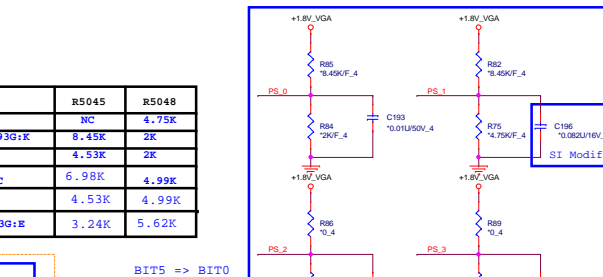
Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

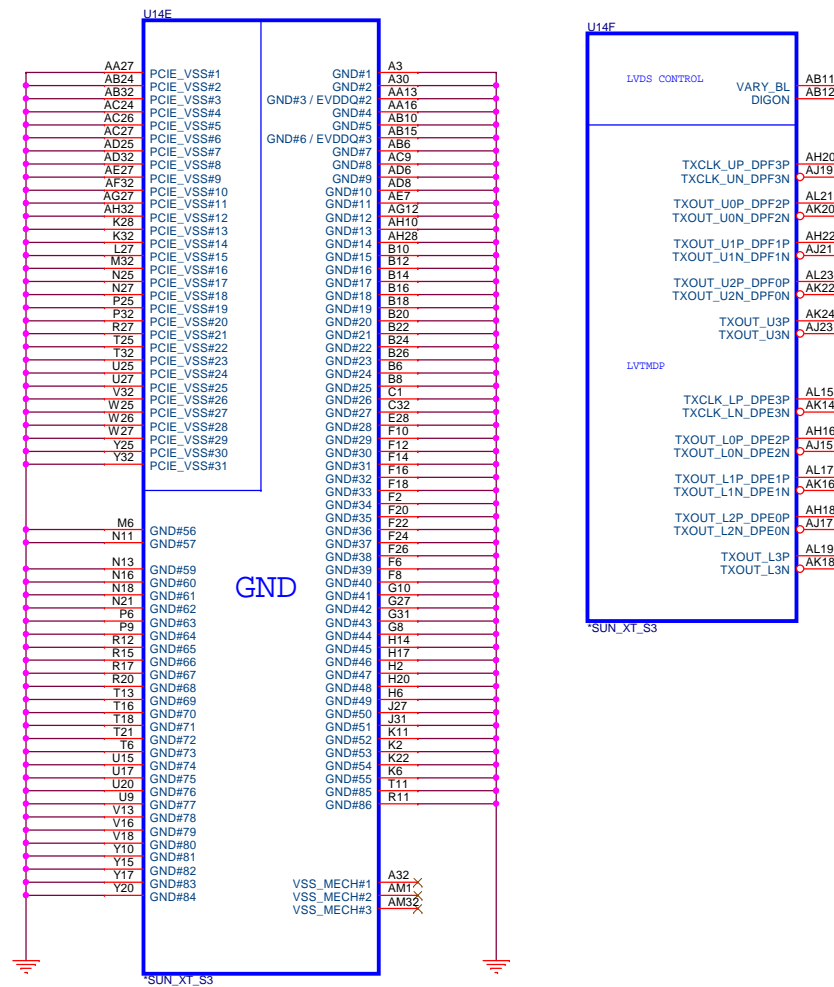
Resistor Divider Lookup Table

R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

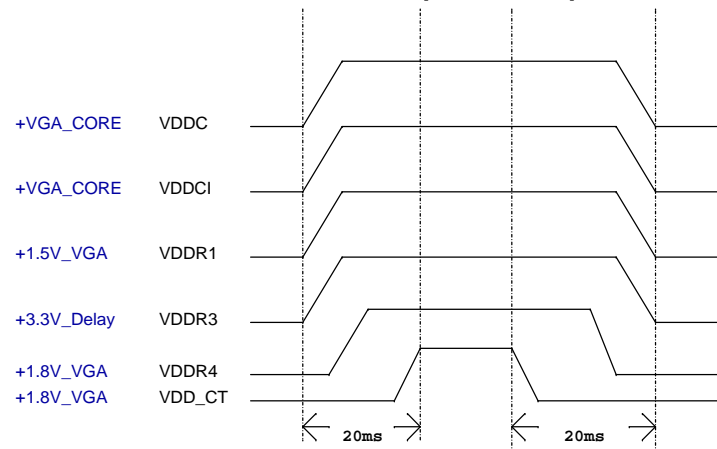
Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved		1 genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwr_srb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_3[3]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

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Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

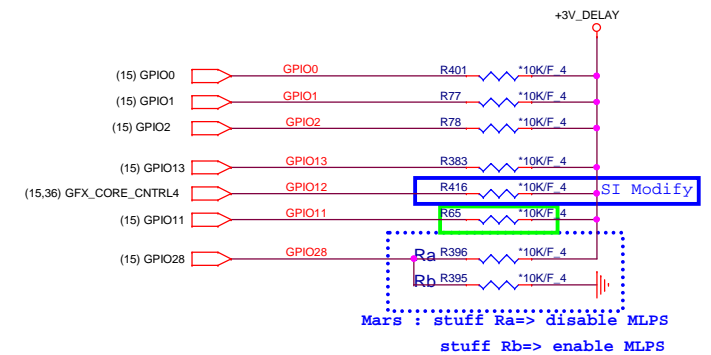
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

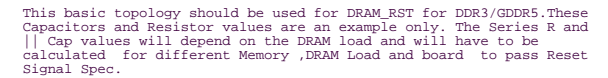
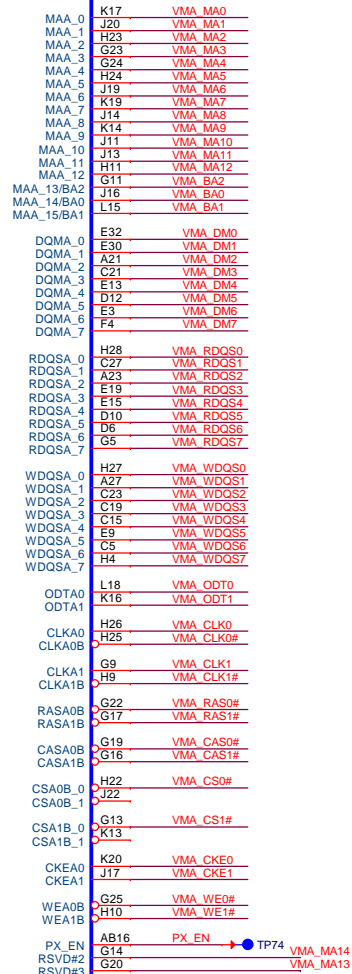
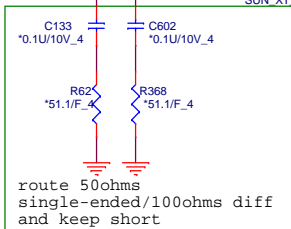
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

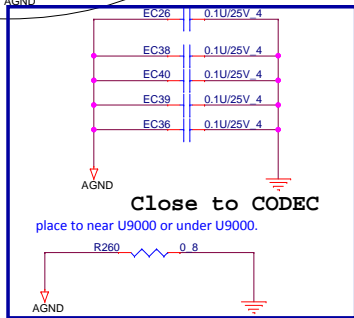
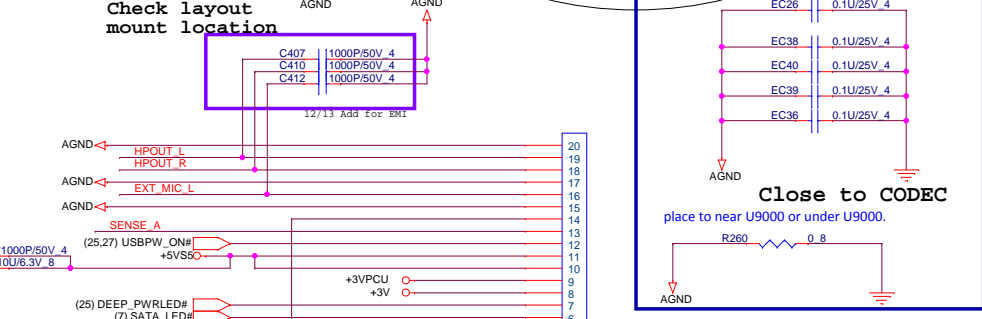
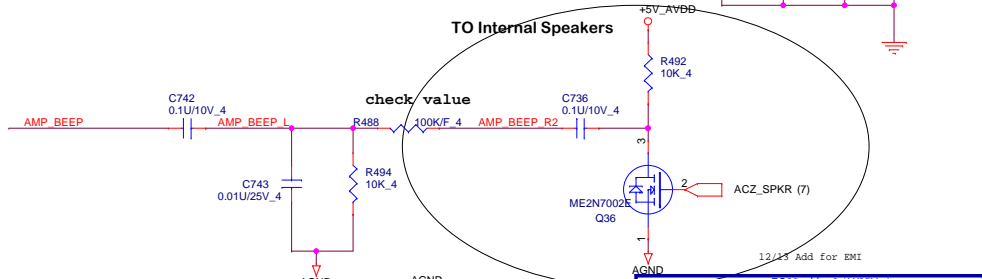
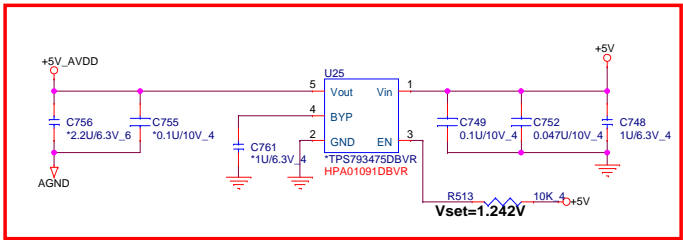
GPIO21 H2SYNC GENERICC GPIO8 GPIO2



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	Sun S3 GND / LVDS/ Straps	
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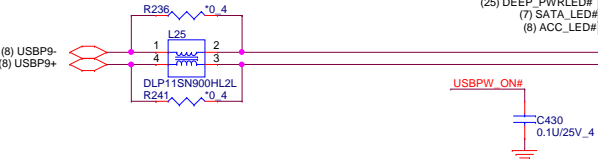



Check layout
mount location

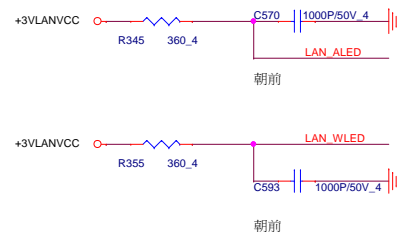
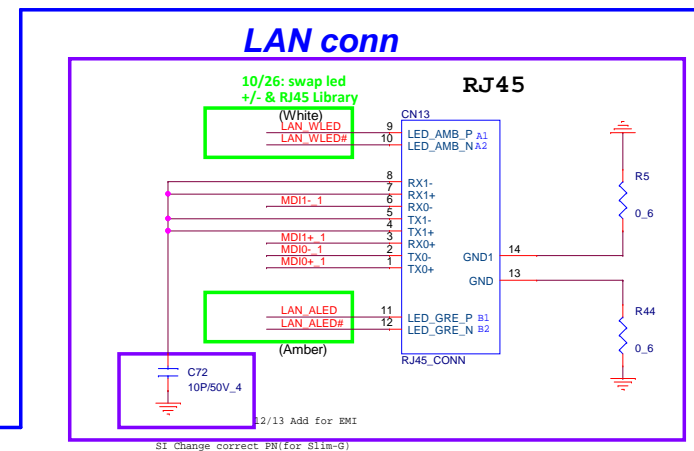
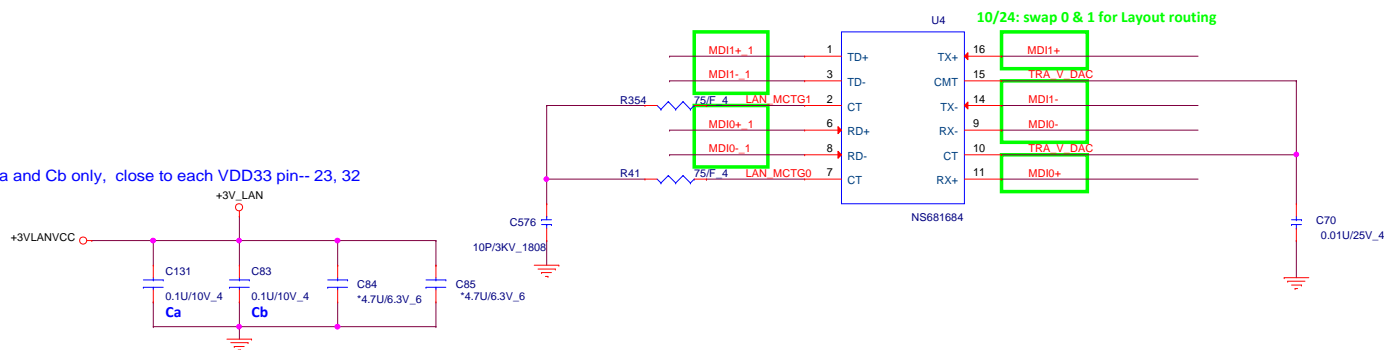
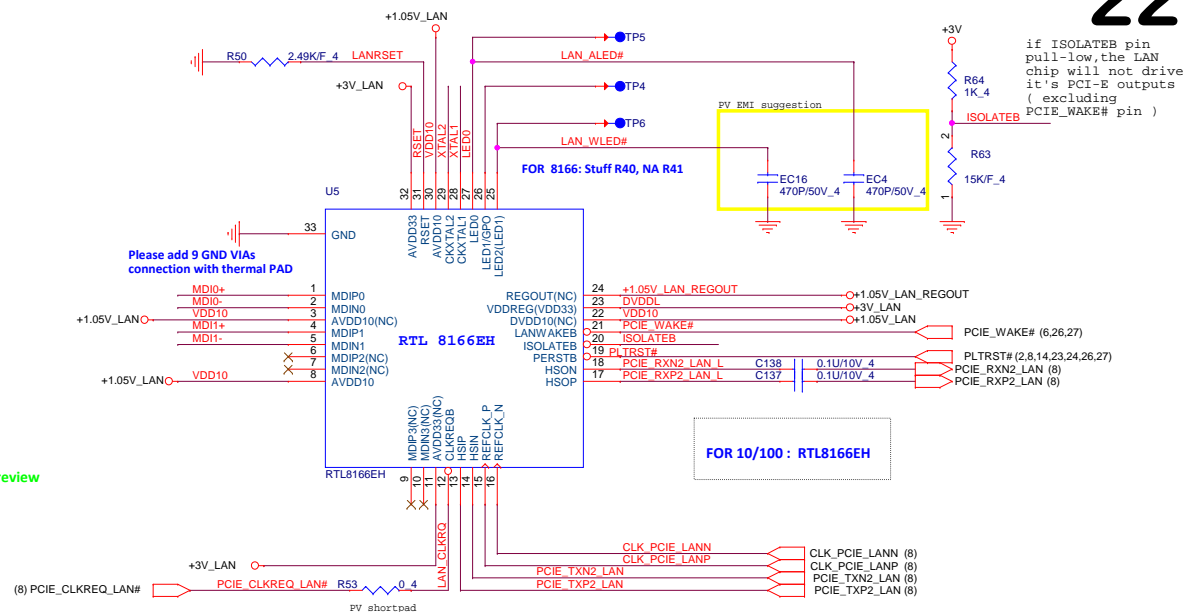
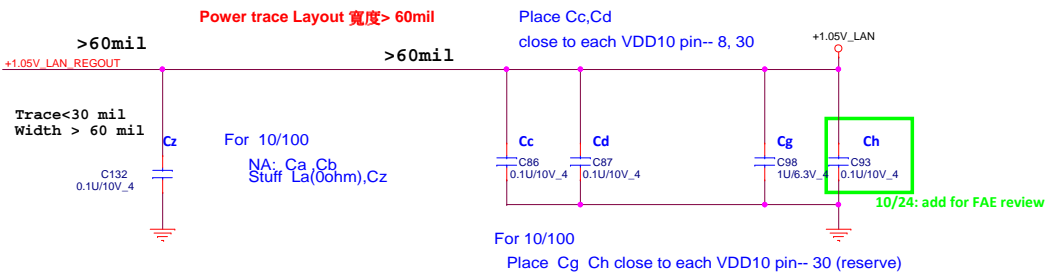
Close to CODEC

Signal	EC23	EC24	EC25	EC26
L SPK+	21000P/50V	4		
L SPK-	21000P/50V	4		
R SPK+	21000P/50V	4		
R SPK-	21000P/50V	4		
ACZ_SDIN0	*33P/50V	4		
ACZ_SDOUT_AUDIO	*10P/50V	4		
ACZ_SYNC_AUDIO	*10P/50V	4		
BIT_CLK_AUDIO	*33P/50V	4		

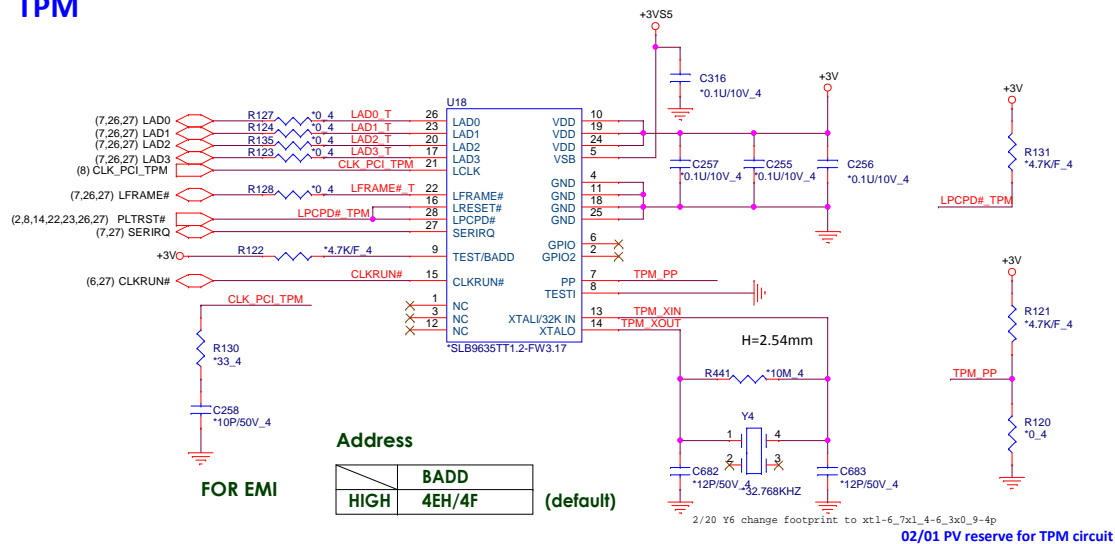
FOR EMI



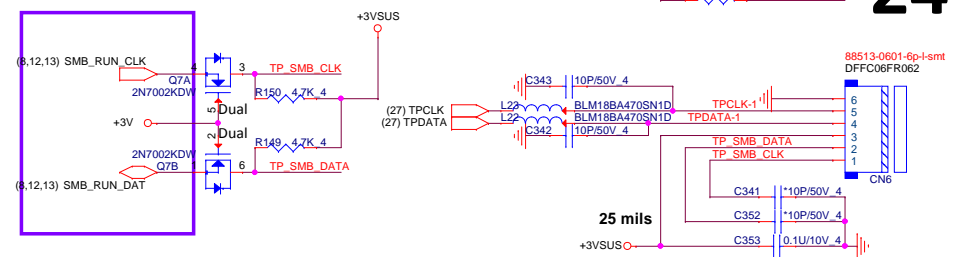
	PROJECT :U81 Quanta Computer Inc.		
	Size Custom	Document Number Azalia ALC 3227/D-MIC	Rev 1A
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TPM

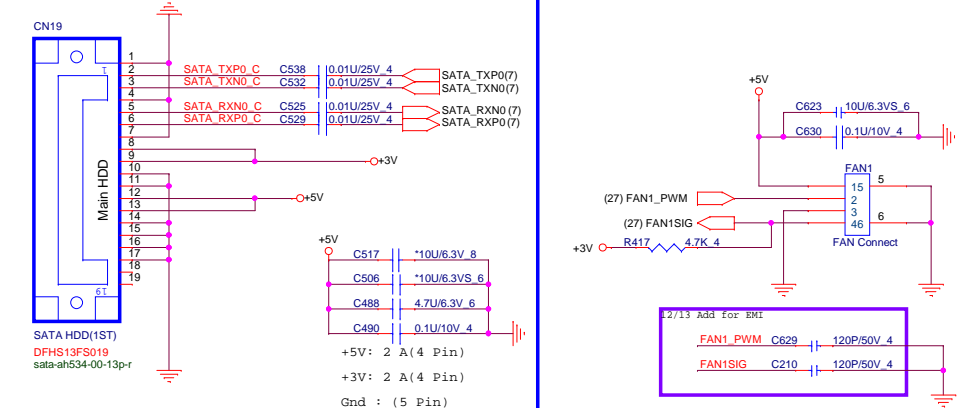


Touch Pad Connector

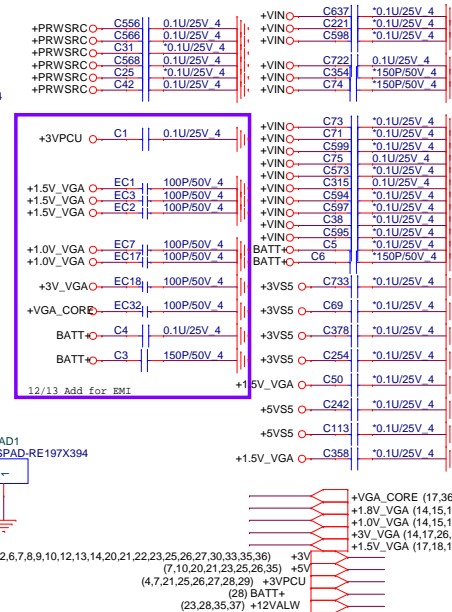
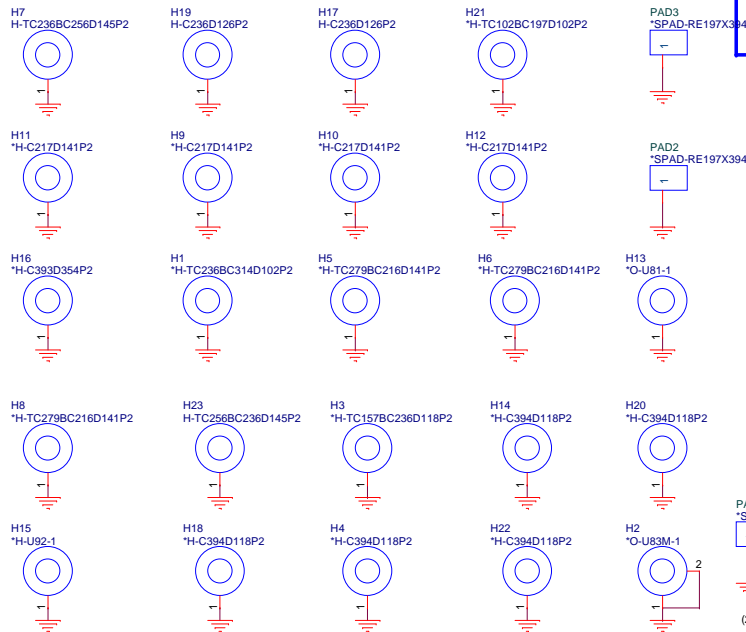


SATA HDD Connector(Cable type)

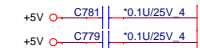
Bypass CAP close conn



Hole

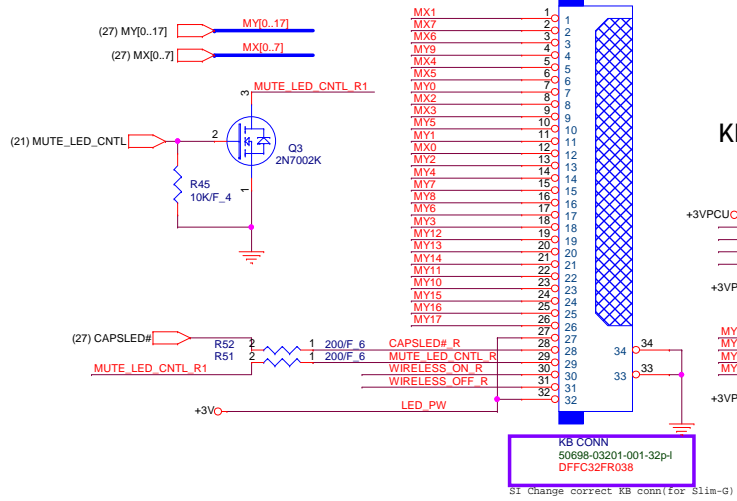


Mini PCI-E Card 2- Full size mSATA

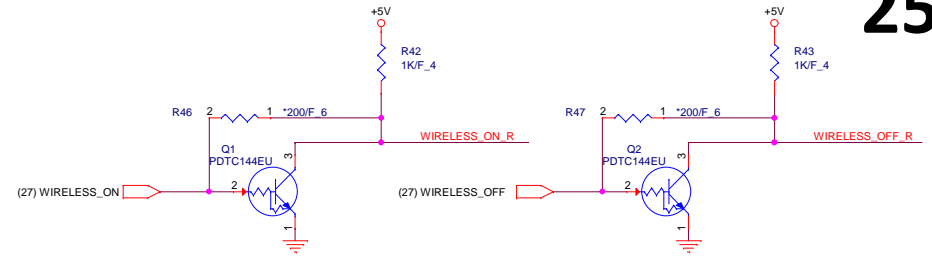
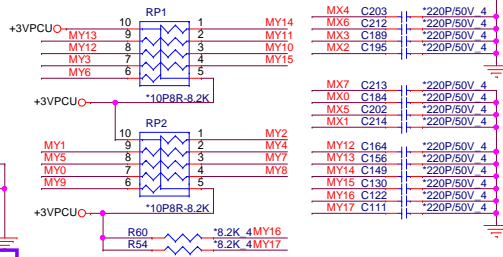


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KEYBOARD Con.

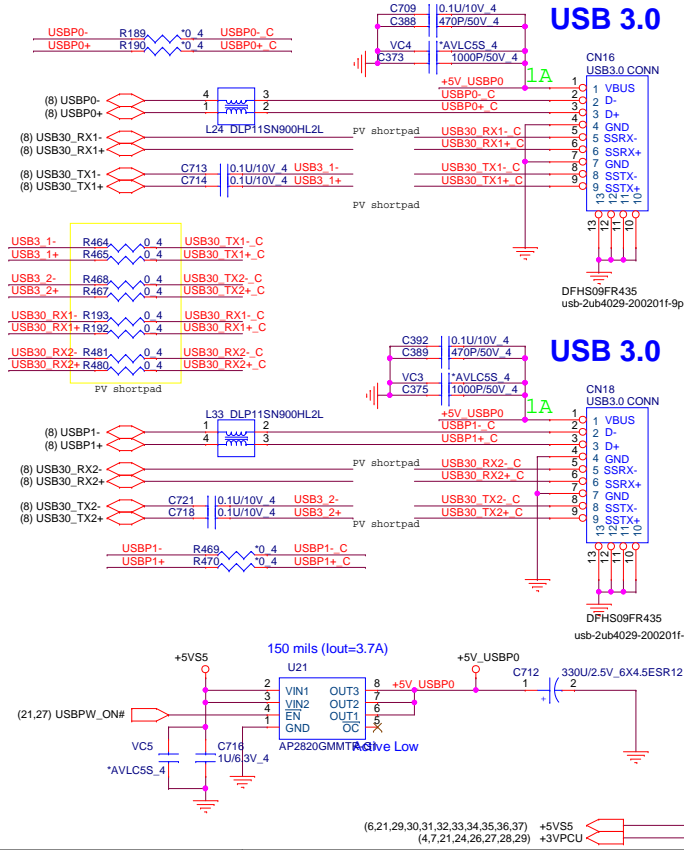
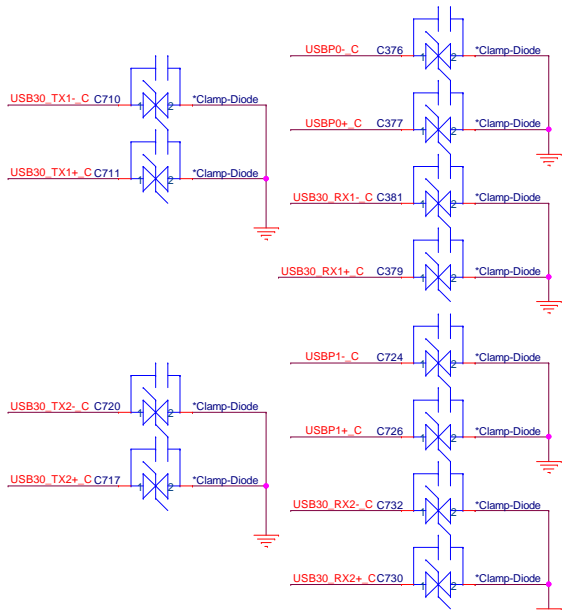


KEYBOARD PULL-UP

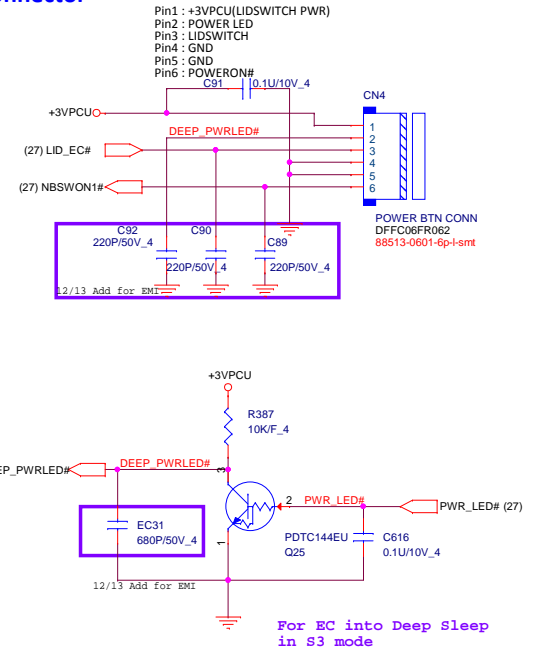


25

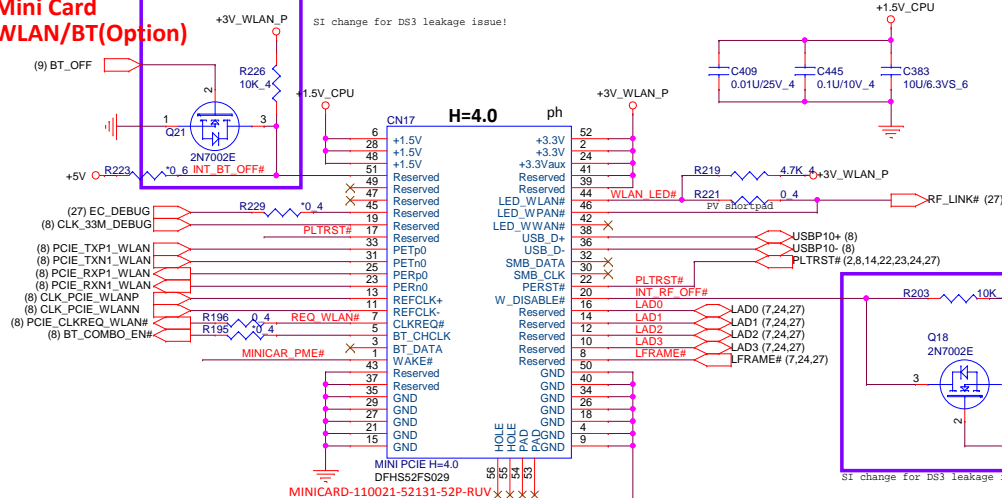
USB 2.0/3.0 Combo



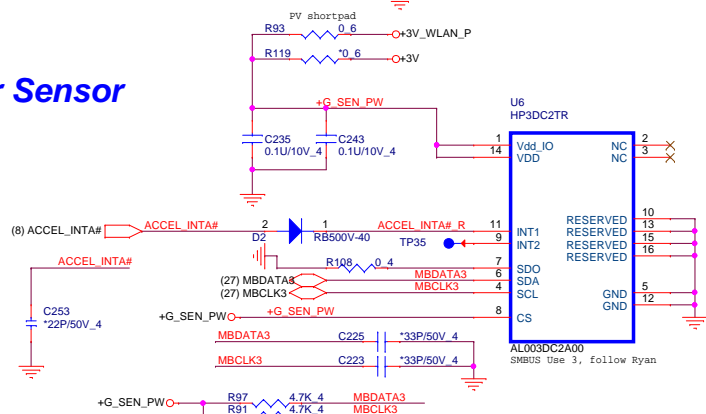
Power Button Connector



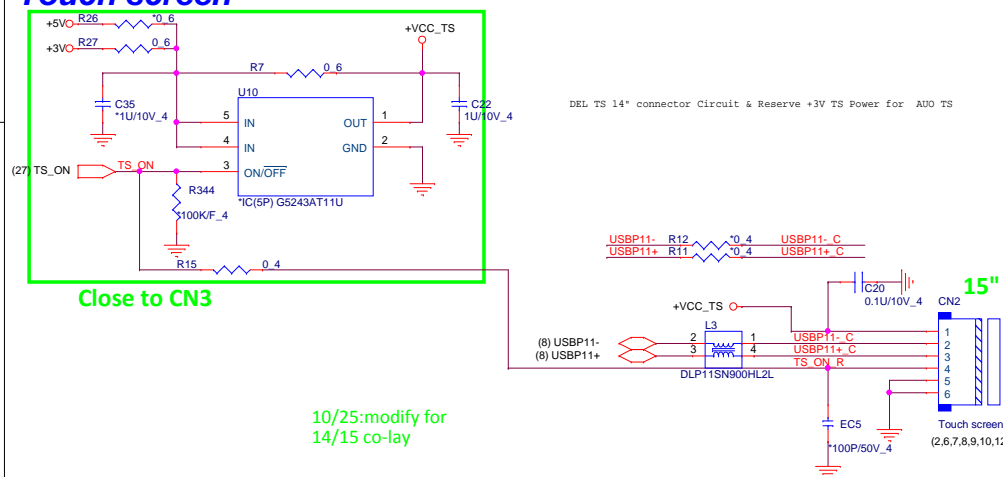
Mini Card WLAN/BT(Optional)



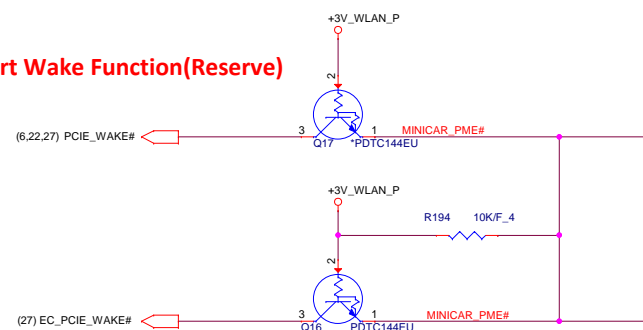
Accelerometer Sensor



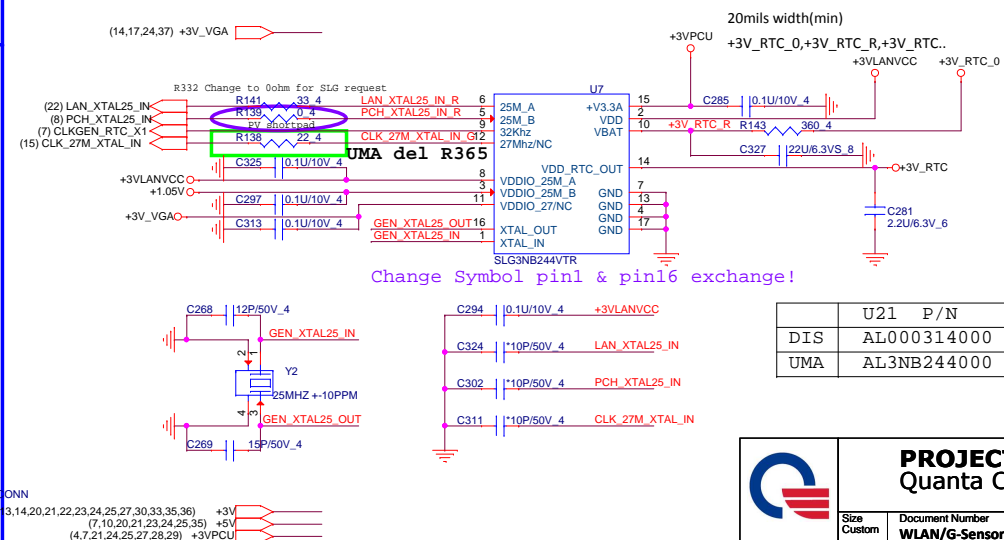
Touch screen



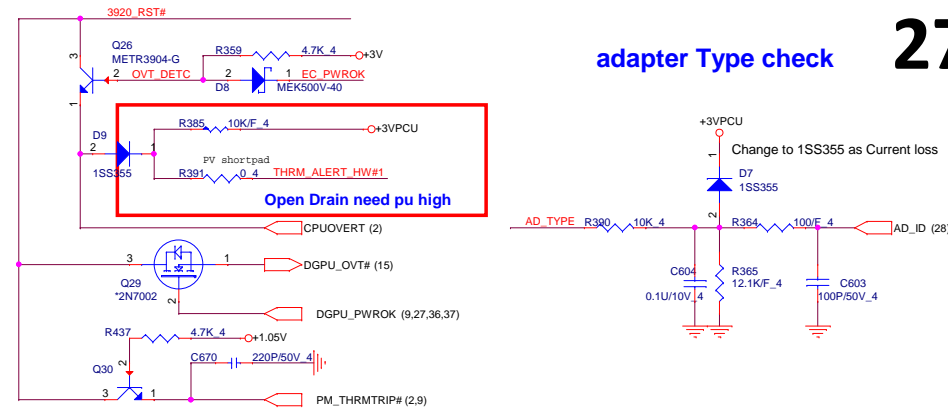
Support Wake Function(Reserve)



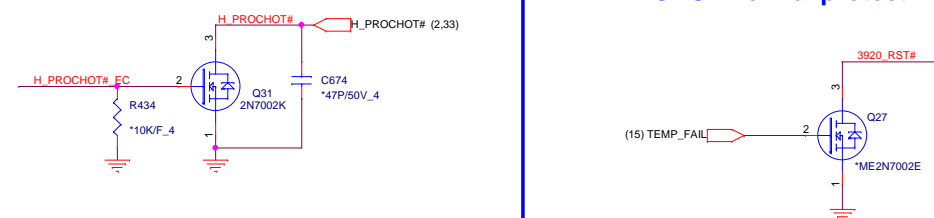
Green CLK Circuitry



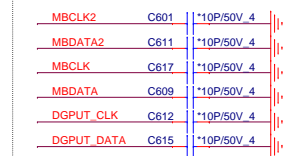
adapter Type check



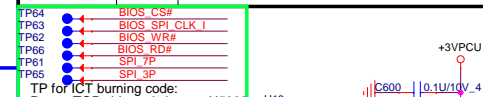
DGPU Thermal protect



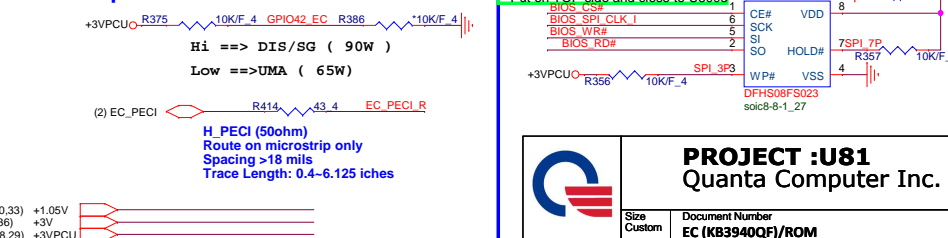
Reserve for ENE Hold time issue



Vender	Size	P/N
EON	1MB	AKE3GZNOQ01 (EON EN25Q80A-100HIP)
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

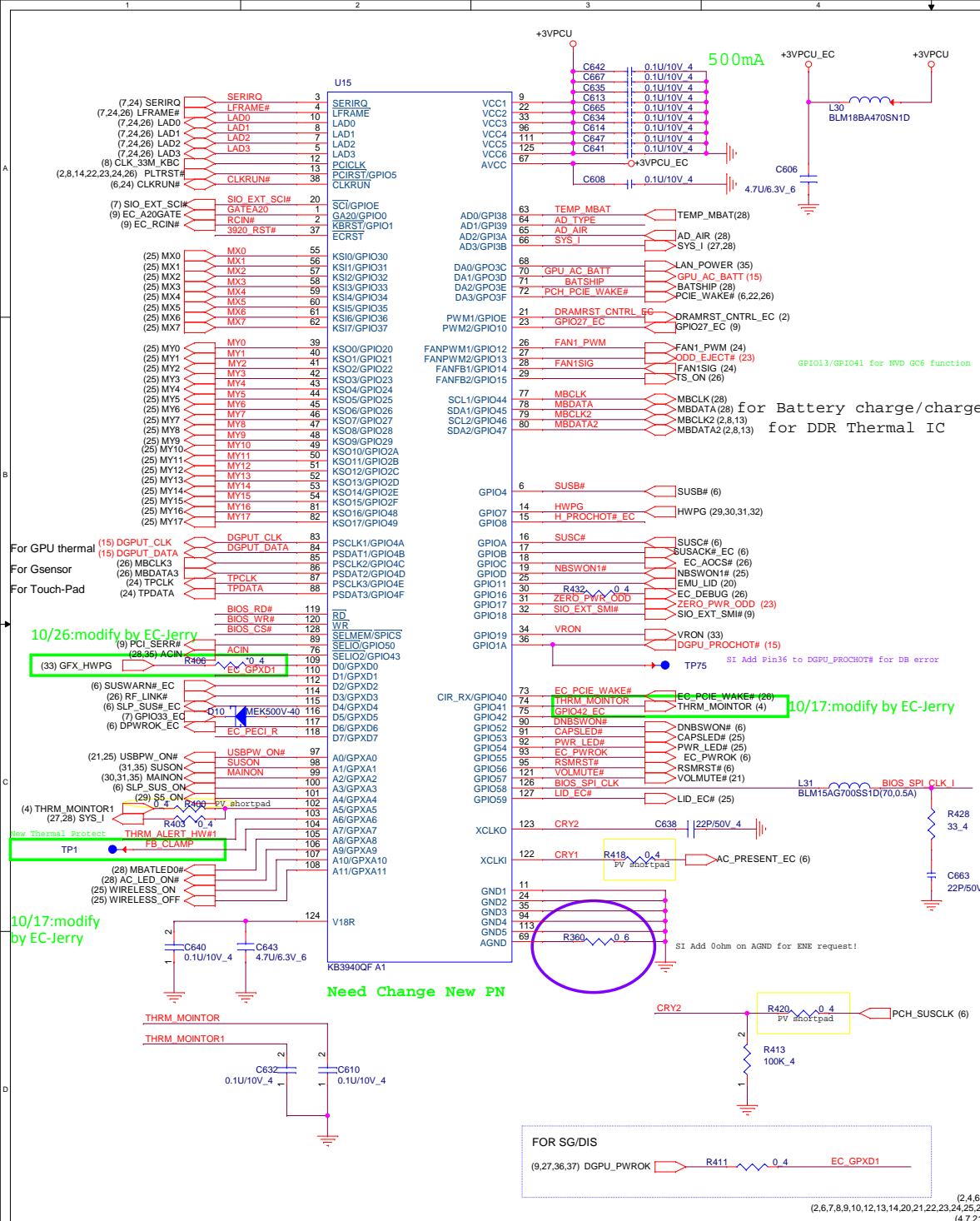


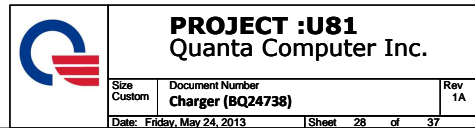
Adapter select for EC



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Custom	EC (KB3940QF)/ROM	1A
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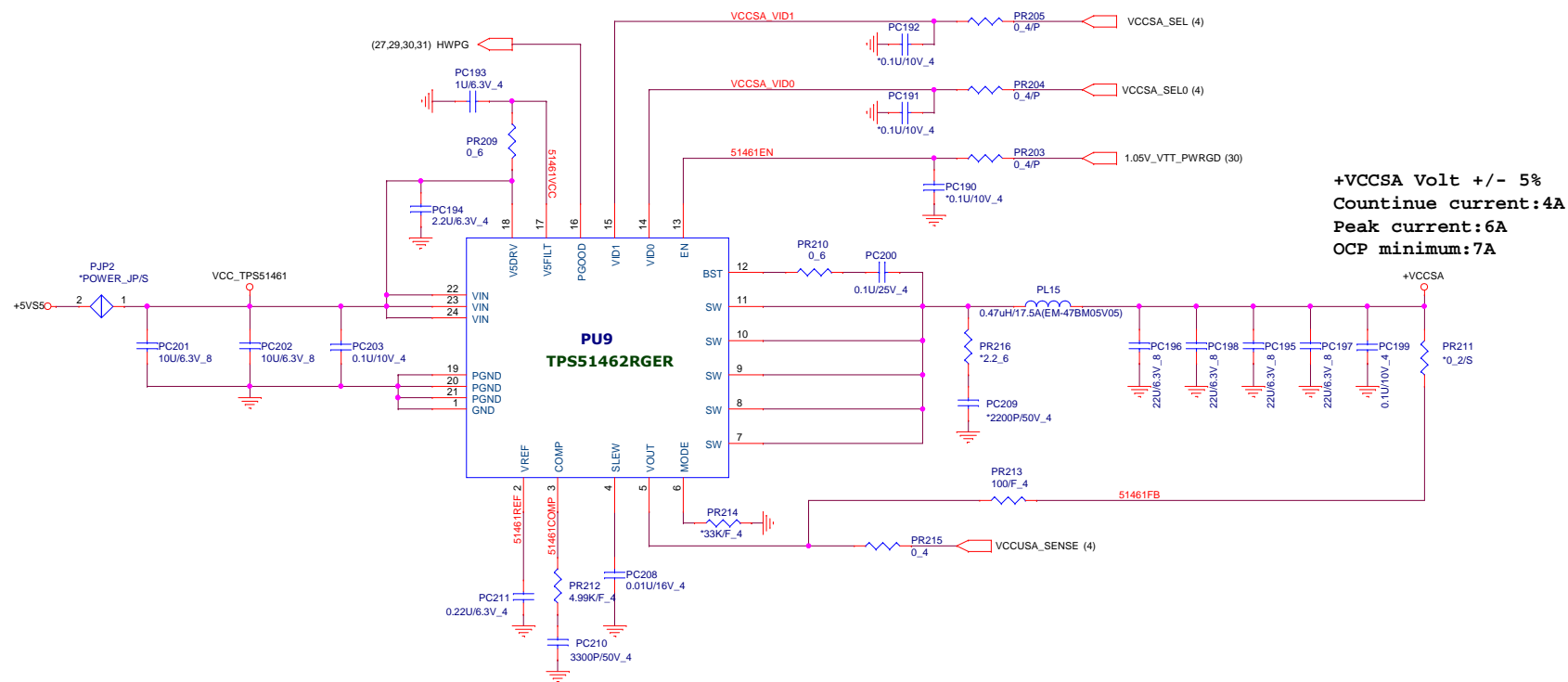


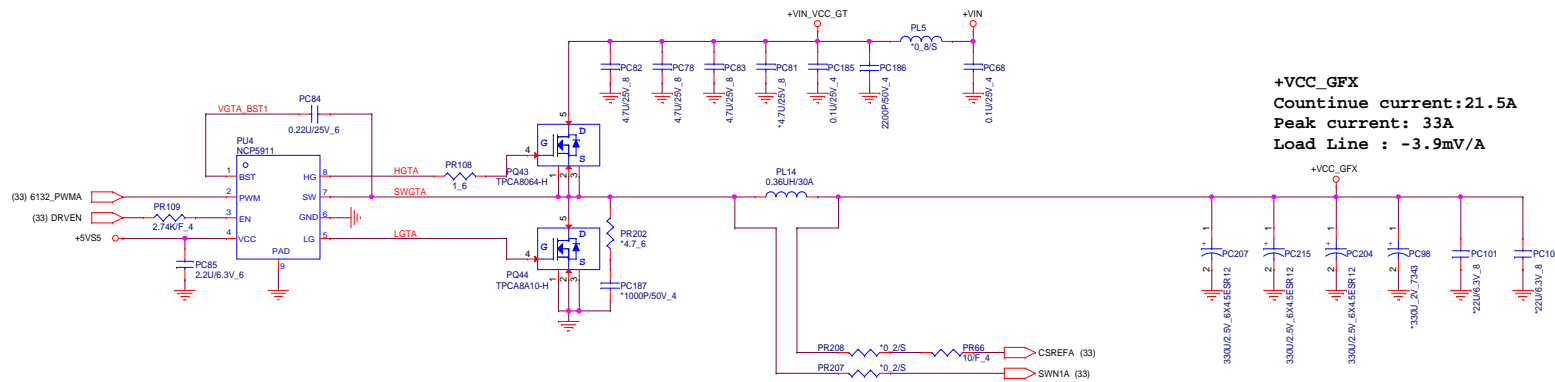
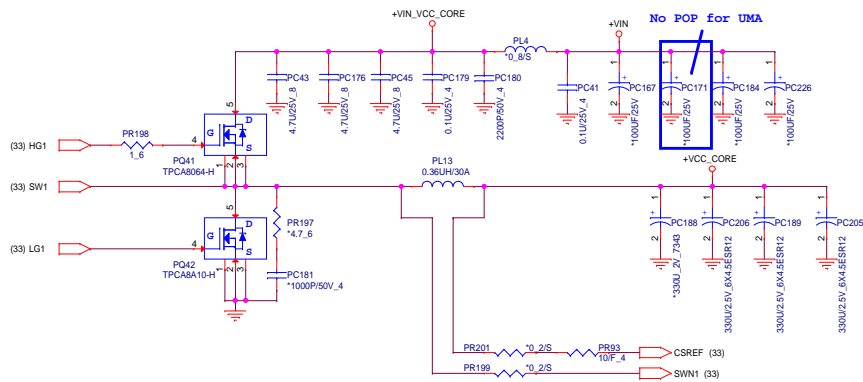


TPSS1462RGER/AL051462000

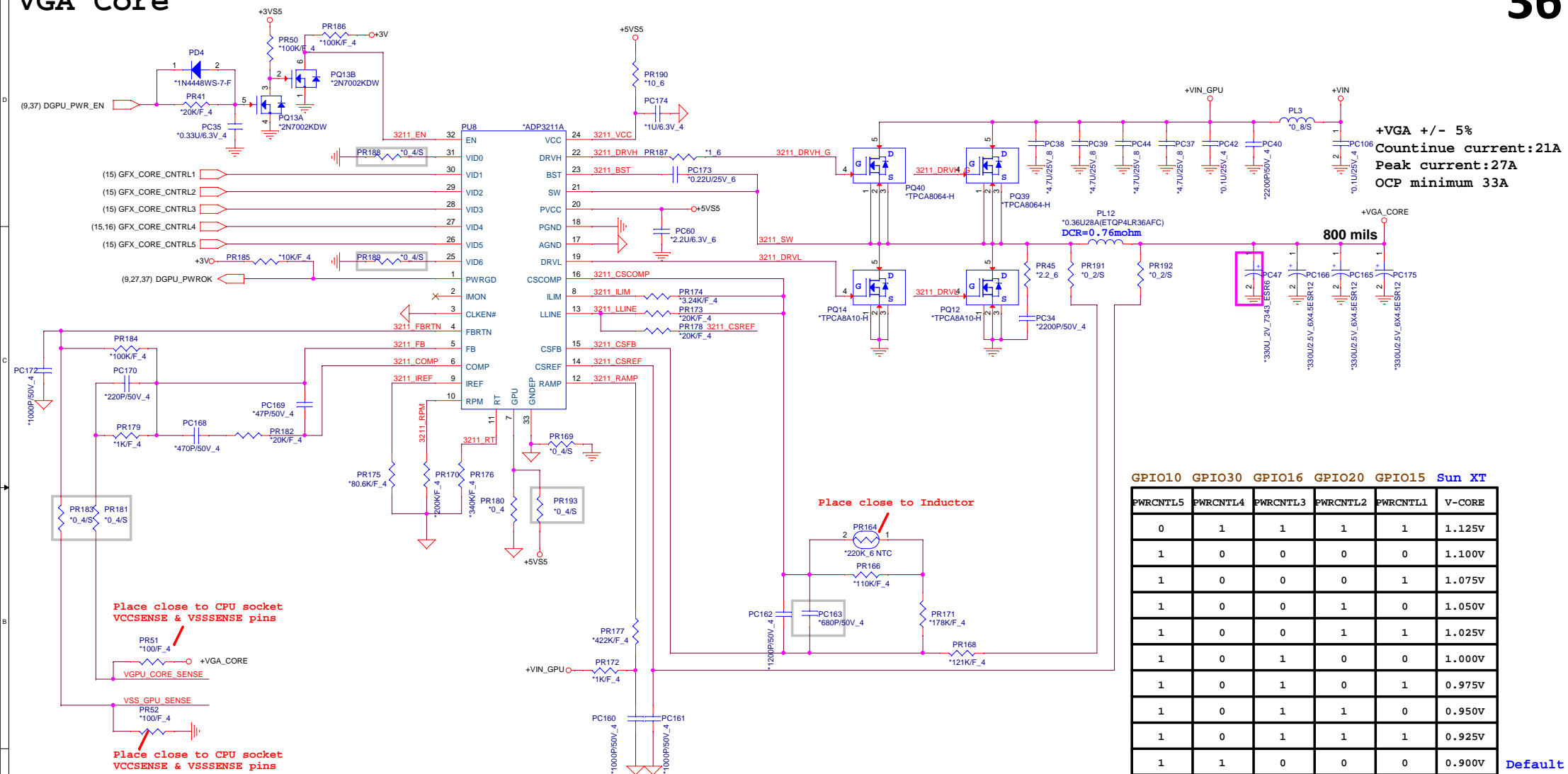
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V





VGA Core



VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A

